EXHIBIT G

JEDEC MANUAL

JEDEC Manual of Organization and Procedure

JM21T

(Revision of JM21S, November 2017)

SEPTEMBER 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.
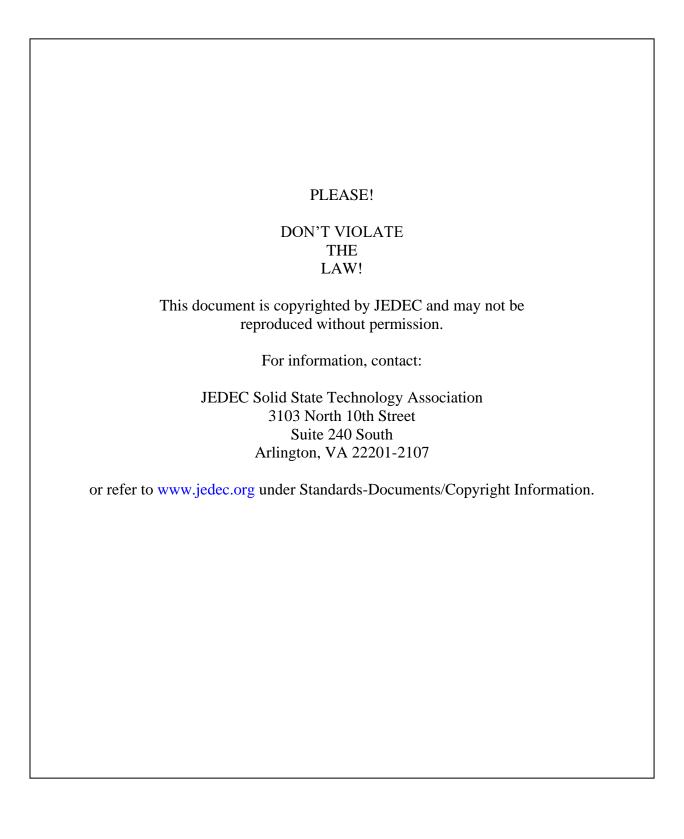
Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2020
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Contact JEDEC

Printed in the U.S.A.

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

Contents

JEDEC Manual No. 21T

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

Contents (cont'd)

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

Contents (cont'd)

JEDEC Manual No. 21T

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

(From JEDEC Board Ballot JCB-02-31A, JCB-04-75, JCB-04-89, JCB-05-60, JCB-05-103, JCB-05-124, JCB-05-99C, JCB-06-02, JCB-06-36, JCB-08-11, JCB-09-65, JCB-09-73, JCB-09-82, JCB-09-86, JCB-10-15, JCB-10-21, JCB-10-88, JCB-12-38, JCB-13-46, JCB-13-47, JCB-15-14, JCB-17-24, JCB-19-04, JCB-19-27, JCB-20-14, and JCB-20-15, formulated under the cognizance of the JEDEC Board of Directors.)

1   JEDEC

JEDEC is an independent incorporated Association governed by a Board of Directors (Board). The Association facilitates standardization within the solid-state, microelectronics, and associated industries, and other related activities through special purpose committees.

The Association and its members are committed to foster open competition in the development of products and services.

1.1   Mission

The mission of JEDEC is to serve the solid state industry by creating, publishing, and promoting global acceptance of standards, and by providing a forum for technical exchange on leading industry topics.

1.2   Scope

The scope of JEDEC includes but is not necessarily limited to areas relating to (1) solid state devices, (2) integrated circuits, (3) electronic modules and associated electronic components, and (4) various manufacturing functions/processes.

1.3   Membership

Any company, organization, consumer, or individual conducting business that itself or through a related entity manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services, shall[1] be eligible for membership in JEDEC. Membership on a given committee shall be open to any JEDEC member company in good standing dependent solely on the dues structure defined by the Board[2]. Government representatives may also participate as described in 2.4.

Each member company, organization, or individual shall be entitled to appoint one member and multiple alternates for each committee it joins. The member and alternates should be capable of making a technical contribution to the standards-setting process of the committee. To preserve the "one-company one-vote" concept within JEDEC, wholly-owned or majority-owned subsidiaries shall not be granted separate voting privileges within any single committee or subcommittee. The JEDEC Office shall maintain a list of all member companies and representatives for each committee.

---

[1] Special word usage. The word "shall" indicates a requirement; see JM7, Annex J.

[2] JEDEC membership is not a prerequisite to committee participation. Non-member participation fees will be charged. Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual. Further details are available from the JEDEC Office. See 3.4.

JEDEC Manual No. 21T
Page 2

1.3   Membership (cont'd)

All changes in committee membership shall be the responsibility of the member company, who shall so advise the JEDEC Office and the committee chairperson in writing or by electronic means.

NOTE   Government regulations restrict the participation of non-U.S. Nationals at certain meetings. Every effort shall be made to notify member companies, well in advance, when a meeting will cover restricted topics.

1.4   Board of Directors

The governing body of JEDEC is the JEDEC Board of Directors (Board) which is comprised of individual Directors (or their alternates) representing JEDEC member companies.

1.4.1   Eligibility

Any maximum dues paying Member Company of JEDEC, having an identified representative in two or more committees for at least the past two consecutive years, may nominate one candidate for Board membership. The nomination consists of the nominee's resume accompanied by a letter from a company executive to the Board chairperson (in care of the JEDEC Office). The support letter is to request that the nominee be considered for Board membership and committing that if elected the member company will support the nominee's active attendance and participation in JEDEC Board meetings and affairs. If the application meets the above requirements, the JEDEC Office will hold the application on file with other (qualified) nominees. The JEDEC Office will maintain an official list of nominations to the Board. A list of the current Board Committees with a brief description and the membership of each will be sent to the nominee with an invitation for the nominee to participate where he/she has interest.

Seats on the Board are occupied by Directors representing individual JEDEC Member Companies. Once elected to a Seat on the Board, the Member Company maintains its position until the seat is voluntarily relinquished or forfeited due to other events as outlined in 1.4.4. Mergers, divestitures, acquisitions and other corporate changes that do not substantially alter the nature of a member company will not be grounds to forfeit a seat on the Board so long as the new entity continues to meet all Board Eligibility Requirements, see 1.4.3.

The total number of Directors shall not exceed thirty (30).

1.4.2   Election of Directors

The Membership Committee (chaired by appointment of the Chairman of the Board with membership open to any Board Member) shall review with the Board circumstances of a vacated seat and recommend qualified nominees from the official nominations list. In order to choose an appropriate nominee to fulfill objectives of the Board, the Membership Committee will review activities that are being conducted in active Board Committees with their respective Chairs.

1.4.2   Election of Directors (cont'd)

The following process will occur:

- Board Committee Chairs will be informed of the vacant seat by the Membership Committee.
- It will be the responsibility of the Membership Committee to qualify the level of support required to achieve ongoing Board Committee objectives.
- The Membership Committee will compile inputs and prepare a review to the Board at the next Board meeting including a recommendation on how to fill any vacated seats.

The following procedures and guidelines will be employed by the Membership Committee during the preparation of its Director recommendations:

- Gathering of Board Committee Chair inputs on current activities and resource requirements. Chairs will have an opportunity to review with the Membership Committee special requirements, shortcomings, etc. that should be made evident during the election process.
- Identification of the nominee's JEDEC experience and previous contributions. Tenure and amount of activity within a Committee or Task group will be identified.
- Identification of Board demographics in regards to representation of committees.
- Identification of the leadership qualities the candidate will bring to the Board.
- Identification of the unique value of the individual and the member company. (Value based on Committee Objectives identified to properly support JEDEC.)
- Identification of the individual's education and professional background (Engineering, Management, Finance, Marketing, Business development, etc.) and the balance the candidate will bring to the Board.

The Board will act on the recommendations of the Membership Committee. New Directors are elected to the Board by a 75% majority of the Board members voting at the meeting. There is no requirement that the maximum of 30 Seats be filled. The Membership Committee will send a response letter to the elected candidate/company and inform them of their responsibilities as outlined in this section. The elected Director's qualifications will be presented in regards to support as an active member on one or more of the Board Committees. The Board may stipulate a contingency period during which the newly-elected Director is required to serve on one or more Board Committees.

1.4.3   Board Representation Changes

The following outlines events that may occur that affect Board Representation.

1.4.3.1 Merger

Two companies on the Board merge or consolidate:

- It is up to the new surviving company (or the new parent company) to decide which Board representative remains on the Board to comply with the "one vote per company" rule.

JEDEC Manual No. 21T
Page 4

1.4.3   Board Representation Changes (cont'd)

1.4.3.2 Acquisition

One Board company acquires another Board company:

- It is up to the acquiring company to decide which Board representative remains on the Board to comply with the "one vote per company" rule.

A Board company acquires a non-Board company:

- The Board company can elect to nominate a different Board representative if it wishes, but final approval is still required by the Board.

1.4.3.3 Merger or Acquisition by Non-Board Company

A non-Board company merges with or acquires a Board company:

- If the non-Board company is eligible for Board membership (ref. 1.4.1), it can assume the Board seat of the acquired company subject to Board approval.

- If the non-Board company is not eligible for Board membership, it cannot assume the Board seat of the acquired company and the Board seat is considered open.

1.4.3.4 Split

A Board company splits into two or more companies:

- If the Board representative associated with the split (or spun-off subsidiary) is still employed by the member company then his/her status is unchanged.
- If the Board representative associated with the split is now a member of the new (or non-member) company then representative in question loses his/her seat.
    - Exceptions: Board decides that the Board representative in question is vital to the Board and the new member company complies with all JEDEC requirements to be on the Board.
- The member company that still has a seat on the Board can nominate a new representative to the Board who is then subject to Board approval.

1.4.4   Member company and Director resignation

The Director will relinquish a position on the Board in the instance of any of the following events:

1) The Member Company formally resigns the position. This includes a statement from the Member Company that confirms the Director and Member Company resignation.
2) The Member Company which the Director represents is no longer eligible as defined in 1.4.1.
3) The Member Company is removed by a majority vote of the Board for gross violation of JEDEC policy.
4) The Director is absent from and not represented by a Member Company's approved alternate at two consecutive Board meetings. It is the expectation that Directors attend all Board meetings, at minimum Directors must attend at least one face-to-face Board meeting, in person, each calendar year.

1.4.4   Member company and Director resignation (cont'd)

In the event that a Director no longer represents the Member Company for which the individual was elected (including but not limited to retirement or change of employment) or should the Director be removed due to gross violation of JEDEC policy outside of the control of the Member Company, then the Board seat shall not be considered vacated and the Member Company shall have the right to maintain its position on the Board by nominating a replacement Director. The replacement Director must meet all nomination requirements as set forth in 1.4.1 and be elected by the full Board by a 75% majority of the Board members voting at the meeting. Should the replacement Director fail to be elected, the Member Company may submit a second candidate and repeat the process.

1.4.5   Officers of the Board of Directors

The officers of the Board shall follow the same guidelines as the officers of a committee with the following exceptions: There shall be at least one Vice Chairperson on the Board. The number of Vice Chairpersons on the Board shall be determined by regular vote at any regularly scheduled Board meeting.

1.4.6   Board of Directors meetings

All meetings of the Board shall follow the same procedures and guidelines as outlined for regular committee meetings, with exceptions per 1.4.6.1, 1.4.6.2, and 1.4.6.3.

1.4.6.1 Board of Directors executive session

The needs of the Association occasionally require the Board to meet in executive session. Such executive sessions are to be defined as closed meetings of Board member company representatives and guests invited for specific purposes only.

1.4.6.2 Board of Directors voting

All actions within the Board require an affirmative vote of at least 75%; members abstaining shall not be considered for determination of the 75% criterion. When defined and agreed to by a duly recorded vote of the Board, specific action may require polling of all members whether present or not and/or may require a higher percentage affirmative vote.

1.4.6.3 Emergency action by the Board of Directors

If action normally requiring Board consideration must be taken, and a meeting cannot be reasonably convened, then the following modifications apply to the approval process: 1) A reasonable attempt must be made to notify 100% of Board members, and 2) The decision shall become binding only upon receipt by the JEDEC Office of affirmative votes from 75% of the members of the Board.

JEDEC Manual No. 21T
Page 6

1.4.7   Board of Directors guest policy

All guests must be approved by the chairman and must have a purpose related to the topics of discussions at the Board meeting. The guest must be introduced to the Board at the meeting and the purpose of the guest's visit should be stated in the agenda for that meeting.

At the discretion of the Board, a guest may be allowed to stay beyond the allotted time slot if the Board feels there is a need for that guest's continued attendance. Otherwise, all guests may only attend the portion of the Board meeting that is directly related to their purpose in the meeting. At no time may a guest speak to the Board beyond the intended purpose of his/her invitation without the explicit approval of the Board.

At anytime, any member of the Board may request that the chairman, at his discretion, ask a guest to leave the meeting.

1.5   Governance/Interpretation

The Board shall have the sole authority to interpret, in whole or in part, these operating procedures. In any case where conflict arises from ambiguity, or lack of specificity, or misunderstanding within or related to this document, the officers of the Board of the Association may make temporary rulings to be confirmed or modified at or before the next regularly scheduled Board meeting by vote of the Directors. In any case where there is not agreement between 100% of the officers of the Board concerning an interpretation, then the matter must be referred to the entire Board for resolution.

1.6   Scope of participation

The standards development process shall not be dominated by any single interest category, individual, or organization. Dominance means a position or exercise of dominate authority, leadership, or influence by reason of superior leverage, strength, or representation to the exclusion of fair and equitable consideration of other viewpoints.

The standards development process should have a balance of interests. Participants from diverse interest categories shall be sought with the objective of achieving balance.

NOTE   In the case of an ANSI American National Standard, JEDEC shall comply with the criteria for balance as contained in ANSI Essential Requirements.

1.6.1   Interest categories

For a formulating group to work effectively, all interest categories should be represented, and no interest category shall be intentionally excluded. Because standards development depends on consensus rather than the will of a majority, participation in the consensus-building process is of far greater significance than the final act of voting in a formulating group. Unless it is claimed by a directly and materially affected interest that a single interest category dominated the standards development process, no test for dominance is required.

Interest categories are defined relative to each standards activity: producer; user; and general interest. See ANSI Essential Requirements for further information.

1.6.1   Interest categories (cont'd)

1.6.1.1 Producer

Producers are formulating group members that manufacture electronic equipment or electronics-related products covered by the standard.

1.6.1.2 User

Users are members that utilize electronic equipment or electronics-related products covered by the standard to provide services to an end user.

1.6.1.3 General interest

General Interest members are neither producers nor users. This category includes, but is not limited to, regulatory agencies (state and federal), researchers, other organizations and associations, end users and consumers.

1.7   Limits and restrictions

The Members (particularly where they are direct competitors in certain lines of business, and including their employees and representatives), shall, when engaged in the activities and affairs of the Association, act in a manner that does not violate any state, federal or international laws or regulations.

Member companies must abide by all applicable export control regulations of their respective countries while attending a JEDEC meeting, irrespective of where the meeting is actually held. It is recommended that the member seek guidance from his or her company if involved in "state of the art" engineering work, as significant changes are made to the export control regulations from time to time.

The Association prohibits any discussion on specific costs, prices, quantity or yield of production levels, methods or channels of distribution, markets, customers or any other topic, or any conduct that may be construed as a violation of antitrust laws. Each respective member company shall advise its respective participant representatives and employees on the importance of compliance with applicable state, federal or international antitrust laws or regulations and require the scope of any discussions or exchanges amongst representatives of Members and/or the Association, be limited to the mission and scope of the Association stated above.

1.8   Modifications to the Manual of Organization and Procedure

Modifications to this manual may be made in whole or in part, upon approval by the Board by the normal ballot process. Any changes to this Manual shall be distributed to the JEDEC membership at the earliest possible time upon adoption.

JEDEC Manual No. 21T
Page 8

---

2   Committees

The Board shall have the authority to establish committees to perform any task(s) for the association. JEDEC committees (main and sub) shall be authorized only by the Board, and the Board shall approve the scope of each[3]. A main committee shall be designated by the prefix JC- plus a two-digit designator, such as committee JC-11. Main committees are separated into two types: (1) service committees, whose scope is limited to a specific subject that may impact several product types, and (2) product committees, whose scope is limited to a specific type product. For service committees, the first digit of the two-digit designator shall be the number 1, and for product committees, the first digit shall be the number 2 or higher.

When the main committee finds it necessary to divide its work into parts, subcommittees may be formed under the scope of the main committee and such subcommittees shall be designated by adding a period to the main committee number followed by a number or a number-and-letter designator (e.g., JC-42.3 or JC-42.3B).

Subcommittees shall have all the same authority and responsibilities as committees herein defined, except that a subcommittee scope shall be a subset of a committee scope, to be authorized, reviewed, and approved by the Board.

NOTE   Participation shall be open to all persons who are directly and materially affected by the activity in question.

2.1   Committee responsibilities

Each committee shall have the authority to consider all matters within its approved scope, including but not limited to the following actions:

a)   Develop proposed standards, guidelines, registrations, and related technical publications for committee ballot.

b)   Authorize committee ballots on all matters within the committee's defined scope.

c)   Initiate proposals for Board ballots of previously approved committee ballots.

d)   Evaluate the results of all committee ballots, as well as comments on related Board ballots.

e)   Request approval of the Board to convert standards or publications into ANSI or IEC standards.

f)   Maintain liaison with other national and international organizations.

g)   Initiate press releases to announce a significant advancement in the work of solid state technology covered within the committee scope such as: registrations, standardization, or publication. All press releases are to be issued by the JEDEC Office after review and concurrence by the JEDEC Legal Counsel.

---

[3] The committee scope shall go through the standard balloting process and must be completed within a reasonable timeframe and prior to any publication of a JEDEC document authored by the committee.

2.2 Executive committee

A JEDEC committee or subcommittee may form an executive committee to manage its administrative work. The executive committee shall meet the following criteria:

a) The executive committee should be chaired by the committee or subcommittee chairperson and shall include as a minimum all chairpersons and vice chairpersons of that committee and its subcommittees.

b) Meetings of the executive committee shall be open to any committee member who gives reasonable advance notice to the executive committee chairperson or secretary.

c) Actions of the executive committee shall be limited to handling administrative matters dealing with such items as meeting schedule, meeting agenda, future meeting dates and locations, personnel requirements, proposed work priorities, and the like. Any decision made by the executive committee is subject to review and modification by the full committee at the request of any committee member or alternate. Decisions on the final disposition of all technical matters shall be made only by the overseeing committee. Recommendations concerning future meeting dates and locations should be presented to the overseeing committee.

2.3 Election of officers

All JEDEC committee officers shall be members or alternates of their respective committees. All JEDEC committees shall have a chairperson and may also have a vice chairperson as officer(s) of the committee. All officers shall be directly elected either by secret vote of the committee members present during a regular meeting or by ballot as determined by vote of the committee. Committee officers shall serve a term of two (2) years. The JEDEC staff shall count the secret ballot and announce the result at the meeting.

At least two meetings prior to the end of a chairperson's term, he/she shall appoint a nominating committee to propose candidates to fill the next term of office(s) for the committee. The committee's candidates must be presented to the full committee at the next meeting and nominations from the floor shall also be accepted. All nominees must agree to accept the additional responsibilities before they can be considered.

If any of the officers cannot fulfill his/her term then elections shall be held at the earliest opportunity of the committee members. Similarly, if a new committee is formed, then the chairperson shall be selected by vote of the members attending the first meeting as a first order of business of the committee. These special case elections shall become effective immediately.

2.4 Government entities

JEDEC desires and encourages the active participation in its standards-developing activities of all parties having a direct and material interest in the standards, including U.S. federal, state, and local government entities when they have such a direct and material interest via the JC-13 Committee, Government Liaison.

Contribution to the standards development process may take the form of liaison with appropriate formulating groups, participation in the ANSI public review process, and active participation in formulating groups.

JEDEC Manual No. 21T
Page 10

3   Meetings

Communication between JEDEC member companies is essential for the work within the Association. All committees shall hold regular meetings for the purpose of conducting JEDEC business.

The use of teleconference or other electronic conferencing equipment is permitted for any type of JEDEC meeting.

3.1   General requirements

Every JEDEC meeting, regardless of type, shall be held in accordance with the directives contained within this manual and in accordance with all applicable laws.

All meeting notices, agendas, ballots, and minutes shall be distributed only by the JEDEC Office. All correspondence from the JEDEC Office shall only be by electronic means unless otherwise required by law. If a company requests distribution by other means, the JEDEC Office will charge a fee for such additional service as directed by the JEDEC Board. The JEDEC website, www.jedec.org, shall be the primary method of electronic communication.

3.2   Notices

Notices of regular meetings shall be distributed solely by the JEDEC Office no less than 28 calendar days prior to the start of such meeting, unless a "special" meeting is authorized by committee vote and the date and agenda for such meeting is fixed at a regularly scheduled meeting. Notices of such special meetings shall be distributed as soon as possible after said regular meeting and in no case less than 10 calendar days prior to the start of such special meeting.

3.3   Agendas

All meetings shall have prepared agendas distributed as soon as possible, but in no case less than 10 days prior to a meeting and should be included with the meeting notice if possible. All special meeting notices shall include the agenda at time of distribution of such notice.

3.4 Meeting attendance

All JEDEC committee and subcommittee meetings are open to members, their designated alternates, and guests invited by the committee or subcommittee chairperson.

A JEDEC staff member or a designated alternate must participate in every committee meeting, either in person or by electronic means. The duties of the staff person shall include but not be limited to taking minutes, advising the chairperson regarding the content of this manual and JEDEC legal policies and guidelines, and distributing the minutes. JEDEC staff attendance is not required at every subcommittee meeting.

A potential new member company may be a guest for one meeting with prior approval of the chairperson. A timely submission of such a request stating the purpose of attendance shall be given so that appropriate accommodations can be made. If there are any issues to be raised by a guest, those issues must be specified in the purpose statement.

Nonmembers may participate in committee meetings if they pay a nonmember participation fee, the fee shall be predetermined, fixed, and reasonable. A procedure for requesting a fee waiver or fee reduction shall be available. Nonmembers do not have the right to vote. Nonmembers should contact the JEDEC Office prior to the meeting date for further details.

Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual.

An individual representative may represent only one company at any committee, subcommittee or task group meeting, and may vote on behalf of only one company on any ballot placed on the electronic voting machine. It is the responsibility of the committee chairman to enforce this rule during a committee or subcommittee meeting. For the electronic voting machine, it is the responsibility of the ballot sponsor to enforce this rule when the ballot tally is reported.

3.5 Quorum

The JEDEC Office shall maintain a list of active members for the sole purpose of determining the quorum requirements for a committee meeting. An active member is defined as a member company that has been represented at either or both of the previous two consecutive regular meetings of the committee. Special meetings shall not be considered for the purpose of determining "active" member status. The quorum requirements shall be 50% by count of a committee's active member list, but in no case shall the quorum requirement be greater than 12 member companies regardless of committee size. All committee member companies present at a meeting are counted toward quorum requirement.

3.6 Recording devices

Voice or video recording devices of any kind are forbidden at any type of JEDEC meeting.

JEDEC Manual No. 21T
Page 12

3.7   Minutes

The principal activities and attendees at all JEDEC meetings shall be duly recorded in meeting minutes. Meeting minutes shall be taken by the assigned JEDEC staff for that committee or by a substitute designated by the JEDEC staff. In the absence of a JEDEC staff person at a committee meeting, a temporary secretary may be assigned by the committee chairperson.

Minutes shall be termed "unconfirmed" until reviewed and confirmed by the committee chairperson and JEDEC Legal Counsel. In the interest of member company needs, minutes should be distributed to members and alternates within 14 calendar days after a meeting. If the chairperson is unable to review and confirm the minutes within that time, the JEDEC Office should distribute the unconfirmed minutes clearly labeled as unconfirmed minutes. Unconfirmed minutes shall be approved by JEDEC Legal Counsel prior to distribution. Confirmed meeting minutes from regular meetings shall be distributed no later than 28 days prior to the next regular meeting. Confirmed minutes from "special" meetings should be distributed as soon as possible after such special meeting and in no case less than 10 days prior to the next regular meeting.

At the end of each set of minutes the following statements shall appear:

"Reviewed/corrected and authorized for release" followed by the Chairperson's and Secretary's name and date.

Chairperson, Name / date

Secretary, Name / date

Confirmed Legal Approval Date

"This meeting was conducted in accordance with JEDEC Legal Guides and the JEDEC Manual of Organization and Procedure."

For those situations where a report from an independent group is included in the minutes, for information purposes, then the following disclaimer may be added to the minutes:

"Disclaimer: All liaison, government, technical, and task group reports contained herein are believed to be accurate but the accuracy or completeness thereof is not guaranteed."

Minutes of a task group meeting shall include a list of the attendees, the meeting agenda, a status review of the agenda items, and any final proposals including discussion related to the proposals. The time, the place, and any required follow-up should be included. Task group minutes are reported and approved as part of the minutes for the next meeting of the sponsoring committee.

3.7.1   Policy statement on JEDEC sign-in/attendance rosters

The policy statements reproduced on the reverse side of the JEDEC sign-in/attendance rosters shall become an integral part of the minutes of all committee, subcommittee, and task group meetings; and a statement shall be included in the minutes indicating compliance with the foregoing policy.

3.8   Regular meetings

Every JEDEC committee shall set up an annual calendar for regular meetings at which any item covered under the scope of the committee may be discussed. Under the JEDEC guidelines, committees must hold at least one (1) regular meeting each year to retain status as an active committee.

3.9   Special (Limited Scope)

All JEDEC committees shall have the authority to approve meetings of limited scope. Schedule for the meeting and specific agenda items must be approved by formal vote during a regular committee meeting. During a limited scope meeting, no other committee business shall be conducted outside of the specific items on the previously agreed to agenda. Items shall not be added to the agenda of a special meeting.

3.10   Joint meetings

3.10.1   Between JEDEC committees

Joint meetings between two or more JEDEC committees may be authorized by agreement of the committees by vote. Selection of the joint meeting chairperson shall occur by vote of the committees' attendees. The joint chairperson shall ensure that all meeting notices, agendas, and minutes are distributed to the relevant JEDEC committees.

3.10.2   Between JEDEC and any non-JEDEC organization

Joint meetings between a JEDEC committee and any non-JEDEC organization are subject to the same requirements as 3.10.1. In addition, JEDEC Legal Counsel shall establish a Memorandum of Understanding (MoU), see 3.10.3, between the organizations and review all release of information from the meetings to any outside person or organization.

JEDEC committees may meet jointly with other organizations or agencies for the purpose of permanent or ongoing liaison. In these cases, those nonmembers attending the committee meeting are expected to pay their proportionate part of the total meeting costs. Apportionment of the meeting costs shall be agreed upon between the committee chair and the representatives of those groups participating in the meeting(s), subject to the approval of the JEDEC Board.

3.10.3   Memorandum of Understanding (MoU) with any non-JEDEC organization

Prior to the formation of a joint meeting/task group with a non-JEDEC committee, a Memorandum of Understanding (MoU) must be in effect between JEDEC and the other organization covering the following items:

a) Balloting procedure (acceptance criteria, resolution of comments, and disapprovals),

b) Patents procedure (including joint ownership),

c) Distribution rights (copyright, use of association logos, available on JEDEC website without charge),

d) Procedures for future revisions of the document(s),

e) Selection of chairperson(s) and appointment of task group membership, and

f) Meetings and related legal requirements (notices, agendas, motions, minutes, costs, etc.).

JEDEC Manual No. 21T
Page 14

3.11   Task groups

A task group may be authorized by any committee chairperson for a specific non-continuing objective. The task group chairperson, appointed by the committee chairperson, shall be a member or alternate of the overseeing committee. Membership within a task group is open to any member or alternate of the committee within which the task group is formed. In addition, members of the task group may also be appointed by the task group chairperson from nonmember JEDEC companies with approval of the overseeing committee chairperson; appointment shall be based solely on ability to contribute to the work; however, all members of a task group shall conduct their work in accordance with this manual.

A task group is not permitted to hold any formal votes or establish any final results relative to standards, publications, or ballots. All task group activities shall be presented to the overseeing committee for review, modification, and approval in the form of reports generated from every task meeting. By duly recorded committee vote, committees may authorize a task group to issue ballots or other specific tasks as required, the specific exception being that committees cannot authorize a task group to conduct a formal vote. A task group must be dissolved upon completion of its objectives.

Scheduling of task group meetings is subject to approval of the sponsoring committee's chairperson, in order to avoid conflict with regularly scheduled meetings.

3.11.1   Joint task groups between JEDEC committees

Joint task groups between two or more JEDEC committees may be authorized by agreement of the committee chairpersons. Selection of the task group chairperson shall be part of this agreement and that chairperson must be a member or alternate of one or more committees involved in the task group. The task group chairperson shall keep all sponsoring committees on the distribution list for all meeting notices, agendas, and reports. Joint task groups between JEDEC committees shall comply with all other requirements for task groups.

3.11.2   Joint task groups between a JEDEC committee and other organizations

Joint task groups between a JEDEC committee and other non-JEDEC organizations are subject to the same requirements as task groups per 3.11. Unless otherwise authorized by the Board and approved by JEDEC Legal Counsel, such joint task groups shall establish a Memorandum of Understanding (MoU), see 3.10.3, in the same manner as joint committees covered in 3.10.2.

4   Document development procedure

The development of all JEDEC documents shall follow the minimum sequential procedure outlined herein.

1) Presentation – initial showing or distribution of material proposed for publication. Presentations may occur at any regular meeting or special meeting if the limited scope and agenda include such information. Presentations may also occur entirely electronically without being at a meeting. An additional showing of material proposed for publication may be required.

2) Motion for ballot – may occur at any time after a presentation. The motion must have a second before being considered for vote. The company agreeing to second the motion for ballot should be willing to accept responsibility for sponsoring the material should the original sponsor be unable or unwilling to do so. The motion for ballot should be discussed after receiving a second and then a formal vote shall be taken.

3) All committee ballots shall be subjected to the committee's editorial process prior to being posted on the JEDEC voting machine.

4) Committee ballot – if approved, material shall be sent out to ballot through the JEDEC voting machine. Details of balloting procedure are covered in section 6.

5) Motion to Board ballot – if a ballot passes and all comments are addressed then a motion may be made to send the material on to the Board for further consideration and approval. Alternatively, the motion to forward the ballot to the Board is unnecessary if the ballot passes by acclamation, see 5.2.

6) Board ballot – when approved, the committee material shall be sent out to ballot through the JEDEC voting machine. Board ballots follow the same procedures as committee ballots, see 6.6.1(c). When reviewing material passed by committee, the Board primarily considers whether due process has been followed.

7) Publication – once proposed material has successfully completed all the above steps and obtained approval through the appropriate balloting processes, it is approved for publication.

8) All JEDEC documents shall be published by the JEDEC Office.

NOTE 1   Steps may be repeated as many times as required to satisfy the wishes of the member companies participating in the process.

NOTE 2   JEDEC Registrations are special-case publications that do not have to be reviewed by the JEDEC Board of Directors, and the registration procedure ends upon the completion of step 4 above.

JEDEC Manual No. 21T
Page 16

4.1   Copyrights

JEDEC owns the copyright to all documents created through JEDEC, and use of that copyrighted material is at the sole discretion of the JEDEC Board.

For the protection of member companies, all JEDEC publications and standards shall be copyrighted. As a precaution, draft proposals circulated for comment and/or vote shall display the symbol ©, followed by the year and "JEDEC". Stapled or bound documents require this designation only on the first page or title page; short documents that may be distributed unstapled shall be so labeled on every page. When final documents are ready for publication, the JEDEC Office shall register the copyright and maintain all appropriate records.

JEDEC member companies may reproduce any JEDEC document for internal use, without restriction. Use of JEDEC material outside of member companies is at the discretion of the Board. Generally, all JEDEC documents are available on the JEDEC website: www.jedec.org.

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, the committee shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC Office, and the standard or publication shall include a reference to such permission as a footnote.

5   Voting

JEDEC shall formally operate under the rule of "One company, one vote" wherein all formal, binding votes will be restricted to one vote per company. Nonbinding fact-finding "straw" or survey votes are not considered formal votes. Unless specifically authorized by the Board, all approval vote counts within JEDEC shall be a minimum of 2/3 of votes cast. All Board approval vote counts shall be a minimum of 3/4 of votes cast. Abstention votes shall not be considered in the calculation.

Votes taken during committee meetings shall be duly recorded in the meeting minutes, and, except for unanimous votes, the vote count shall be included in those same meeting minutes.

In order to maintain fairness within every committee, the committee chairperson shall refrain from voting during a meeting for all but secret votes. If a chairperson has a specific company position on a topic being discussed, then control of the meeting should be turned over to the vice chairperson or other less biased member. Chairpersons may vote on any ballot to represent his/her company position.

5.1   Ballot voting

The period for voting on committee ballots shall be at least 21 calendar days from the date of issuance, and shall not exceed 90 days. In any case, the ballot closes at midnight, Eastern Time, on the final day of the voting period. All committee ballots shall be processed through the JEDEC electronic voting machine, and shall include the following vote options:

a)   approve, comments are optional with approval

b)   disapprove, comment is required and shall include a full explanation of the reason(s) for the disapproval

c)   abstain, comments are optional with abstain

NOTE   All committee ballots shall contain the following patent statement:

"If anyone receiving this ballot is aware of any patents (granted or pending) involving in this ballot, check here and notify the committee, citing the applicable patent numbers."

No one can have access to the ballot results before the voting period ends. As part of the deliberative, consensus-building process, commenters may send questions to the ballot sponsor independent of their votes via email, telephone, etc.

5.2   Ballot approval by acclamation

A committee ballot is considered approved by acclamation in either of the following two cases:

a)   The ballot is approved unanimously with no comment at the close of the voting period.

b)   The ballot is approved by count at the end of the voting period, and all comments whether from approve, disapprove, or abstain votes are resolved to the satisfaction of the sponsor and the commenting company. If any company is not satisfied with the proposed resolution of a comment, then resolution of the ballot must await committee action.

Any ballot approved by acclamation shall automatically advance to the next level in the publication process (i.e., committee ballots are automatically submitted to the Board, or Board ballots automatically become approved for publication). At the discretion of the committee chairperson, ballots that otherwise meet the requirement for approval by acclamation may be referred back to committee for further action if special conditions exist (e.g., uncharacteristically low vote count for the committee).

JEDEC Manual No. 21T
Page 18

---

6   Ballots

All committee ballots shall be distributed ONLY by the JEDEC Office with Board-approved electronic distribution methods to all committee members and alternates for vote and to all related committees for information and comment. A submission for ballot shall be made through the JEDEC Office ONLY by Board approved editable and non-editable "soft copy" format of the complete ballot content.

Reference to any individual(s) and/or member company name(s) is prohibited from appearing on any committee ballot unless it is part of a return address.

In order to facilitate document identification and retrieval, keywords shall be submitted with all ballots. A keyword is defined as a word, term, or acronym that is descriptive of the essential contents of the ballot or a major portion thereof.

6.1   Editorial changes

During a committee meeting, provided there is no disagreement within the committee that the changes are editorial, these changes may be incorporated into committee-approved balloted material without reballoting.

6.2   Ballot lobbying

Member companies should not lobby or coerce other member companies to approve or disapprove ballots. Open discussion of balloted material is permitted and encouraged, but such discussions should focus on the technical aspects of balloted material.

The use of verbal, physical or business threats, intimidation, harassment or coercion is unprofessional behavior and unacceptable conduct at or in connection with any activity sponsored by JEDEC, including committee and task group meetings.

6.3   Copyrights

See 4.1

6.4   Regular committee ballot

A "regular" ballot is one in which the entire standard, publication, registration, guideline, or specification is open for comment.

Prompt consideration shall be given to the written comments and objections of all participants during the committee balloting process. An effort to resolve all expressed objections accompanied by comments related to the proposal under consideration shall be made, and the disposition of each such comment or objection and the reasons therefore shall be documented in writing (including electronic minutes and ballot material).

6.5 Limited committee ballot

If a limited number of revisions to an existing document are being proposed, a "limited" ballot may be issued. Limited ballots may be restricted to considering only the proposed areas for modification, addition, or deletion. In the cases of limited ballots both the original material and the proposed revisions thereto shall be clearly shown in the ballot material. Examples of appropriate occasions for using limited ballots are (1) a proposal to add a new definition to a long list of definitions or (2) a new package outline to JEDEC Publication No. 95.

On occasion, after a committee ballot has been approved, the committee may wish to propose minor technical changes to the ballot before forwarding the approved material on to the Board for final consideration. In such cases, a motion may be made for a limited ballot in which only these technical changes may be addressed. If the limited ballot is passed, these changes shall be incorporated. If it fails, the original material stands as approved.

NOTE   This process is not intended for use in the development of an ANS.

6.6 Board of Directors ballot

In general, all ballots originating at the Board level shall follow the same guidelines outlined in 6.4. Board ballots are restricted in scope to non-technical Association business and specifically may not include new technical for publication creation as such material must first be submitted by the appropriate technical committee.

6.6.1 Committee ballots sent to the Board of Directors

All passed committee ballots relating to proposed JEDEC standards, guidelines, or specifications must be reviewed and approved by the JEDEC Board before becoming official JEDEC publications. Upon approval by acclamation or by committee vote[4], the originating committee shall submit such passed committee ballot[5] to the JEDEC Office for distribution as a Board ballot.

All ballots submitted to the JEDEC Board must include the committee ballot material, and:
a)   a brief description of the recent committee background regarding the material.
b)   the complete voting report including the names and votes of the member companies voting and all comments on the material.
c)   a description of the resolution of all of the comments on the material. Negative votes must be addressed, however if they cannot be resolved, the ballot can be submitted to the Board with the approval of the committee.

The Board may make only editorial modifications to any material proposed by committee for further action. Any technical modifications of committee material must be referred back to the originating committee for possible action.

---

[4] Unless the committee ballot passes by acclamation, a formal committee vote must be taken and recorded in the minutes to send the committee ballot to the Board for further action.
[5] Ballot material submitted for a Board ballot must be identical to the ballot material approved by the committee. The committee may authorize an editorial committee to review the document for editorial corrections only prior to issuing the Board ballot. In this situation, the Board ballot must be a marked up version of the committee-approved ballot material, such that all edits are clearly noted.

JEDEC Manual No. 21T
Page 20

6.7 Survey ballots

Surveys may be issued to determine whether a proposal warrants further action. A survey may ask for information or for a support/nonsupport position. No committee vote is required for the distribution of a survey ballot; however, every survey must be approved by the committee chairperson and issued by the JEDEC Office following legal approval. The JEDEC Office shall monitor every survey to ensure adherence to JEDEC legal guidelines. Surveys that contain company-sensitive material that must remain confidential shall be stripped of any reference to a company by the JEDEC Office prior to use of the material. In all cases, survey results shall be presented to the full committee at the first meeting following the voting period expiration date.

Survey ballots are for gathering information or further clarifying member positions and survey votes are strictly nonbinding. All surveys should contain the following background statement:

"Companies are under no obligation to respond to this survey."

The committee shall determine the method of data collection to ensure company confidentiality if required. In the case of anonymous surveys, the names of respondents shall be deleted by the JEDEC Office. The survey shall specify the method of data-collection.

7 JEDEC documents

JEDEC documents are available from the JEDEC website: www.jedec.org. JEDEC documents may not be sold without written authorization from JEDEC.

7.1 Interpretation

Official interpretations involving technical matters pertaining to JEDEC and/or ANSI/JEDEC standards and publications shall be made by the formulating committee of the document in question.

7.2 Document Maintenance

JEDEC documents shall be reviewed by the formulating committee within five years of the last publication date, after which the committee shall take one of the following actions with respect to the standards material:

a) Reaffirm it as a JEDEC document
b) Recommend its revision and reissuance as a JEDEC document
c) Recommend its rescission
d) Recommend its consideration as an ANSI or IEC document proposal.

7.3 Document Types

7.3.1 Standards (JESD)

Documents that are intended to represent a sound approach to product specification and application.

7.3.2 Publications (JEP)

Documents containing general engineering information on products, procedures, or services, that are not necessarily appropriate for standardization.

7.3.3 Specifications (JES)[6]

Documents prepared specifically to facilitate procurement, that clearly and accurately describes the essential technical requirements for purchased material or services.

7.3.4 Registered Outlines/Standards (CO, DO, GS, MO, MS, etc.)

Mechanical package outline drawings that have been registered and assigned a JEDEC registration number.

7.3.5 Registration Data Formats (RDF)

Engineering information in the form of a list of specific electrical and mechanical parameters necessary for the characterization of a particular class of solid state devices.

7.3.6 Manuals (JM)

Documents that describe internal JEDEC policies and procedures.

7.3.7 Joint Documents (J-STD, JP, and JS)

Documents created in cooperation between JEDEC and another organization.

7.3.8 ANSI/JEDEC Standards

At the request of the sponsoring committee and after approval by Board ballot, JEDEC standards and publications may be submitted to ANSI through the JEDEC Office for processing as an ANSI National Standard. The JEDEC Office will be responsible for providing appropriate documentation to ANSI. All policies and procedures set forth by ANSI per the "ANSI Essential Requirements: Due Process Requirements for American National Standards" shall be followed. See Annex D for more details.

---

[6] This document type has not been in use by JEDEC since early 1990's but is maintained here for historical purposes only.

JEDEC Manual No. 21T
Page 22

8   Legal guidelines

All meetings of the JEDEC Board and its associated committees, subcommittees, task groups, and other units shall comply with JEDEC Legal Guidelines incorporated herein by reference. JEDEC Legal Counsel may advise the Board and committees from time to time concerning interpretation of Legal Guidelines.

8.1   JEDEC documents and publications

Prior to publication, the following documents including, but not limited to, all JEDEC standards, publications, manuals, minutes, surveys, questionnaires, press releases, registration data formats, and workshop proceedings, formulated by the Board, committees, and subcommittees, must be approved by JEDEC Legal Counsel.

8.2   Patent Policy

8.2.1   Terms and definitions

Affiliate: An entity owned or controlled by a Committee Member, or which controls or is under common control with a Committee Member for so long as such control exists.

NOTE   For purposes of this definition, control means the ownership of greater than 50% of the voting securities of that Committee Member.

Approval by the Committee: An approval by vote of the committee to send a proposed Standard to the Board of Directors for review and approval. Some committees approve proposed Standards in parts, for example, by a "pass-hold" process. In those instances, "Approval by the Committee" means preliminary or final approval of the relevant part of a proposed Standard by a committee vote.

Committee Member: An entity that participates in a JEDEC committee and its Affiliates.

Contribution: Any submitted material, proposal or other submission offered by a Committee Member in the process of developing a Standard for the purpose of incorporating such submitted material, proposal, or other submission into a Standard, provided that such submitted material, proposal, or other submission either, a) exists in a tangible form of expression (including in electronic media); or b) is a verbal statement that is memorialized in written documentation (such as a proposed Standard or submitted material) and is either confirmed or not objected to by such Committee Member within thirty (30) calendar days after its receipt of or access to such memorialization, including without limitation, via posting on the JEDEC website.

8.2.1   Terms and definitions (cont'd)

Disclosure of Potentially Essential Patents (to Disclose Potentially Essential Patents)**:** Disclosure to JEDEC, in writing, in the following form:

a)   for issued patents, disclose the patent owner, assignee (if available at time of disclosure) name, address and intellectual property rights ("IPR") contact person; name or title of the patent; the patent number; the country or countries of issuance, and the Standard(s) on which the submitter of the disclosure believes an Essential Patent Claim may read,

b)   for published applications, disclose the patent application owner, assignee (if available at time of disclosure) name, address and IPR contact person; name or title of the patent; the patent application number; the country or countries of filing, and the Standard(s) on which the submitter of the disclosure believes an Essential Patent Claim may read, and

c)   for unpublished pending applications, disclose the name or title of the patent application, the patent application owner or assignee (if available at time of disclosure) name, address and the IPR contact person; the patent application number; the general subject matter of such unpublished application(s) and the Standard(s) on which the submitter of the disclosure believes an Essential Patent claim may read. Nothing herein precludes broader disclosure of unpublished patent applications on a voluntary basis or pursuant to a non-disclosure agreement.

Disclosure of a patent is deemed to include all patents claiming priority of a single filing. The listing of foreign equivalents is optional and at the discretion of the patent holder.

NOTE   If any of a Committee Member's disclosed patent or patent application contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, the Committee Member must also note this fact in its disclosure statement.

Essential Patent: A Patent containing one or more Essential Patent Claims.

Essential Patent Claims: Those Patent claims the use of which would necessarily be infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard.

NOTE   Essential Patent Claims do not include Patent claims covering aspects that are not required to comply with a JEDEC Standard, or are required only for compliance with sections that are marked "example," "non-normative," or otherwise indicated as not being required for compliance, or related to underlying enabling technologies or manufacturing techniques not specified in the standard.

Participate (Participated, Participation): (a) joining a JEDEC committee or task group involved in the development of or amendments to a Standard; or (b) attending more than one meeting of such committee or task group (in person or by telephone) within a one-year period. "Participate" includes being present at any point in a meeting of a committee or task group even if the individual or entity has not formally joined the committee or task group.

Patents: All classes or types of patents other than design patents (including, without limitation, originals, divisions, continuations, continuations-in-part, extensions or reissues), and applications for these classes or types of patents throughout the world.

Potentially Essential Patent: A Patent that is reasonably believed by a subject person to contain one or more Essential Patent Claims.

JEDEC Manual No. 21T
Page 24

8.2.1   Terms and definitions (cont'd)

Potential Licensees: All JEDEC Committee Members and non-members.

RAND: Reasonable and non-discriminatory licensing terms and conditions.

Representative: An individual who represents a Committee Member. The term includes entities that have not formally joined the committee or task group, if they participate.

Standard: Standards include publications and package outlines, provided that they are adopted (or intended to be adopted) by the JEDEC Board of Directors and have the effect of Standards. Standards work includes activities in JEDEC committees and task groups.

NOTE   Standards include both proposed and adopted JEDEC technical specifications.

8.2.2   General Provisions

8.2.2.1 Committee Members

All Committee Members, as a condition of committee membership or committee Participation, agree to abide by JEDEC rules and procedures, including this JEDEC patent policy ("Patent Policy"). This commitment also applies to entities that Participate in JEDEC Committees or task groups, whether or not they have formally joined as JEDEC members.

All Committee Members, as a condition of committee membership and participation, agree to Disclose Potentially Essential Patents, as set forth more fully in 8.2.3, and to offer to license their Essential Patent Claims to all Potential Licensees on RAND terms and conditions, if and as consistent with 8.2.3 and 8.2.4.

The disclosure and licensing obligations of Committee Members and Participants are limited to Standards developed in the particular JEDEC committees in which and while they Participate.

As JEDEC members, Committee Members and Representatives are encouraged, but not required, both to disclose their Potentially Essential Patents and to license their Essential Patent Claims on RAND terms and conditions for Standards developed in all other JEDEC committees in which they are not Committee Members. Such disclosure shall be in the format described in 8.2.3 and be made to the JEDEC Legal Department.

Committee Members and Representatives are encouraged, but not required, to disclose the Potentially Essential Patents of other entities, including other Committee Members and third-parties.

Committee Members and Representatives are encouraged, but not required, to bring Patent Policy issues or concerns with respect to the Disclosure of Potentially Essential Patents and the licensing of Essential Patent Claims to the attention of the JEDEC Board of Directors for resolution, see 9.2.

8.2.2   General Provisions (cont'd)

8.2.2.2 Committees

JEDEC committees and task groups shall not consider any matters or proposals that are outside the approved scope of such committees or task groups. Furthermore, JEDEC committees and task groups are encouraged to use best efforts to avoid proposals for Standards that are within the approved scope of such committees and task groups and that would be likely to cause Committee Members to terminate their membership in the committee or task group for the purpose of discontinuing their disclosure or RAND licensing obligations.

JEDEC committees and task groups shall keep track of all notices, disclosures and licensing assurances with respect to Potentially Essential Patents and to review, on a periodic basis, the list of prior disclosures of Potentially Essential Patent Claims.

JEDEC committees and task groups shall consider reasonable workarounds and technical alternatives (but are not required to implement such workarounds or alternatives) within the earlier of: a) balloting, or b) one-hundred twenty (120) calendar days of receiving Notice of Refusal to offer Licenses on RAND Terms.

JEDEC committees and task groups are encouraged, but not required, to resolve patent policy issues before balloting. Unresolved issues relating to Potentially Essential Patents may be submitted to the JEDEC Board of Directors for resolution, see 9.2. The sole remedy for any issues or concerns about deviations from approved scope shall be an appeal to the JEDEC Board of Directors made prior to Approval by the Committee, see 9.2.

8.2.3   Disclosure of Potentially Essential Patents

At each committee meeting, the chairperson should call to the attention of all those present the requirements contained in the JEDEC Legal Guides and the obligation of all Representatives to inform the committee of any personal knowledge they have of any Potentially Essential Patents that are owned or controlled by that Committee Member and to call for the Disclosure of Potentially Essential Patents by Representatives. Annex A provides information to be displayed at the beginning of the committee meeting to satisfy the requirement. Additionally, all Representatives should be asked to read the statement attached to each JEDEC sign-in/attendance roster; see Annex A for patent policy application guidelines.

All Committee Members must Disclose Potentially Essential Patents, known to their Representative(s) to be Potentially Essential Patents that are owned or controlled by that Committee Member to the personal knowledge of the Representatives. However, neither Committee Members nor Representatives shall have any obligation to conduct a search for Potentially Essential Patents.

Disclosure of Potentially Essential Patents by a Representative or the Committee Member being represented shall be made as early as reasonably possible. The Disclosure of Potentially Essential Patents shall be in accordance with the definition of Disclosure of Potentially Essential Patents, see 8.2.1. Initial disclosure by a Committee Member or Representative may be made in a meeting of the committee or task group. The Representative is responsible for ensuring that such disclosure is properly recorded in the meeting minutes.

JEDEC Manual No. 21T
Page 26

8.2.3   Disclosure of Potentially Essential Patents (cont'd)

The Representative or Committee Member shall document all known Potentially Essential Patents in either: a) License Assurance/Disclosure Forms, see Annex A.3, or b) Notice of Refusal to offer Licenses on RAND Terms forms, see Annex A.4. Such disclosures or notices of known Potentially Essential Patents shall be delivered to the JEDEC Legal Department within thirty (30) calendar days of Approval by the Committee in order to be effective.

8.2.3.1 Disclosure of unwillingness to license work of a committee

If a Committee Member knows that it would not be willing to offer to license Essential Patent Claims arising from the Contributions of another Committee Member on RAND terms to all Potential Licensees consistent with 8.2.4, the Committee Member shall notify the committee chair in writing as early as reasonably possible but no later than thirty (30) calendar days after Approval by the Committee in the form of a Notice of Refusal to offer Licenses on RAND Terms, see Annex A.4.

The committee shall consider working around the material or other technical alternatives with a goal of resolving the concern if at all possible. The Committee Member may (at its own discretion) withdraw its notification of Refusal to License at any time. However, if the Committee Member wishes to maintain its position that it would refuse to License the work of the committee, the Committee Member must withdraw from the committee no later than one-hundred twenty (120) calendar days after providing notice of its unwillingness to license.

8.2.4   RAND Patent Licensing Commitment

Subject to the terms and conditions of section 8.2.4, each Committee Member, as a condition of Participation, agrees to offer to license on RAND terms, to all Potential Licensees, such Committee Member's Essential Patent Claims for the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard issued during the period of membership in that committee. The licensing commitment does not apply to Essential Patents of a Committee Member where notice of a Refusal to License has been given by the Committee Member in accordance with 8.2.3.1.

This commitment applies to any Standard that was pending in the committee or task group while the Committee Member Participated in that committee or task group. If a Committee Member terminates its committee membership, the commitment does not apply with respect to any new proposal or Standard introduced in the committee or task group after the Committee Member provided notice to the JEDEC Legal Department terminating its committee membership.   If and as necessary, questions whether or not a particular proposal is a new Standard or merely a continuation of a prior Standard will be addressed in the first instance by the JEDEC Legal Department in accordance with 8.2.10.

Certain exceptions apply to the licensing requirement. A Committee Member will not be required to license or continue to license its Essential Patent Claims to a Potential Licensee for a particular Standard if: (i) such Potential Licensee does not agree to grant a license to all other Potential Licensees under such Potential Licensee's Essential Patent Claims of that Standard on RAND terms and conditions for the approved Standard and/or (ii) such Potential Licensee has commenced or has threatened to commence patent litigation targeting such Committee Member's products that are meant to comply with that Standard.

8.2.5   Licensing Assurance/Disclosure Form

A Committee Member or Representative agrees to offer the following licensing options for an Essential Patent Claim:

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments:

(i)   A license will be offered, without compensation, under reasonable terms and conditions that are free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard, subject to the terms and conditions in 8.2.4; *or*

(ii) A license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination, subject to the terms and conditions in 8.2.4.

Such assurance shall indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee[7], and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.

The assurance shall also indicate that it is intended to be binding on successors-in-interest regardless of whether such provisions are included in the relevant transfer documents.

If a Committee Member, at its discretion, elects not to submit a License Assurance/Disclosure Form (see Annex A.3) at or before the time the ballot closes and does not otherwise provide notice of an unwillingness to license in accordance with 8.2.3.1, the Committee Member and its Affiliates will be deemed to have agreed to offer to grant licenses on RAND terms and conditions for all of its Essential Patent Claims of the balloted Standard, if and as consistent with 8.2.4.

8.2.6   Reference to patented products in JEDEC standards and publications

The following notice shall be included inside the front cover of all JEDEC Standards in which Essential Patent Claims are or may be involved:

"The user's attention is called to the possibility that compliance with this document may implicate the use of an invention covered by patent rights."

"By publication of this document, no position is taken with respect to the infringement or validity of any patents. However, JEDEC has received statements of a willingness to offer to license certain rights on reasonable and nondiscriminatory terms and conditions to applicants desiring to obtain such a license. Details may be obtained from JEDEC."

---

[7] Committee Members and Representatives may comply with (i) and (ii) by notifying the transferee in writing that the RAND licensing obligations under Section 8.2.4 are binding on the Committee Member or Representative, the transferee and subsequent transferees or a general statement in the transfer or assignment agreement that the Patent Claim(s) being transferred or assigned are subject to any encumbrances, e.g., a RAND licensing obligation, that may exist as of the effective date of such agreement.

JEDEC Manual No. 21T
Page 28

8.2.7   Special legal disclaimer

The Board has the discretion to approve the issuance of a standard for which a patent owner or applicant has not provided written assurance that the Essential Patent Claims will be licensed, subject to special legal disclaimers.

When determining whether to approve the issuance of such a standard, the Board shall consider whether the committee used diligent efforts, if appropriate under the circumstances, to develop a standard that does not require the use of the Essential Patent Claim(s).

A special legal disclaimer might include the following language:

> "Notice: JEDEC has received information that certain patents or patent applications may be essential to this standard. However, as of the publication date of this standard, no statements regarding an assurance or refusal to license such patents or patent applications have been provided. JEDEC does not make any determination as to the validity or relevancy of such patents or patent applications. Anyone making use of the standard assumes all liability resulting from such use. JEDEC and its members disclaim any representation or warranty, express or implied, relating to the standard and its use."

If the Board determines that:

(1) the claim by the patent owner or applicant that an identified patent or patent application may be essential to implement a Standard is a reasonable claim, and

(2) there is a credible indication that the patent owner or applicant is unwilling or unable to grant licenses, with or without compensation, on RAND terms,

then the Board *shall not* approve the issuance of the standard except as provided in 8.2.7. In its discretion, the Board may seek the advice of an independent outside patent attorney or consultant in making the determinations in subsections (1) and/or (2) of 8.2.7.

8.2.8   Miscellaneous

The Patent Policy applies equally to situations involving the Essential Patent Claims that are discovered after adoption of the Standard.

JEDEC makes no representation as to the reasonableness of any terms or conditions of the license agreements offered by such patent rights holders, and all negotiations regarding such terms and conditions must take place between the individual parties outside the context of JEDEC.

To the extent that Potentially Essential Patent Claims are disclosed with respect to a JEDEC Standard, information regarding the parties who have asserted patent rights in the Standard may be obtained from the JEDEC Corporate Office.

It is possible that other patent rights that have not been disclosed to JEDEC may be implicated by implementation of or compliance with a JEDEC Standard. JEDEC is not responsible for identifying patent claims for which a license may be required in order to implement a JEDEC Standard, and takes no position and conducts no inquiries with respect to the legal validity or scope of those patents or patent claims that are brought to its attention.

8.2.9   Violations

If a Committee Member or Representative materially violates this Patent Policy and the violation is not cured within thirty (30) days following notification of the violation by the JEDEC Corporate Office, the JEDEC Board of Directors may in its discretion suspend the Committee Member or Representative's right to participate in JEDEC. If the Committee Member is allowed to continue participation and engages in another material violation of this Policy, the JEDEC Board of Directors may in its discretion revoke the Committee Member or Representative's right to participate in JEDEC.

8.2.10   Interpretation and Governing Law

The obligations and rights of parties to this agreement in the conduct of committee meetings and the approval of standards as set forth in this Patent Policy will be interpreted in the first instance by the JEDEC Legal Department. When specifically requested by a Committee Member or Representative, interpretations by the Legal Department will be in writing.

Written interpretations by the Legal Department can be appealed by a Committee Member or Representative to the JEDEC Board of Directors. The Board of Directors will make a final decision on appeal, as determined in their reasonable and good faith judgment. The final decision will be in writing.

In no event will JEDEC or the JEDEC Board make a determination that a Patent is or is not a Potentially Essential Patent or that a Patent Claim is or is not an Essential Patent Claim.

The Patent Policy will be interpreted and governed under the laws of the State of New York.

---

9   Appeals

All appeals related to standard or publication development are initially directed to the JEDEC Office. The provision for appeals is important for the protection of all parties involved within the JEDEC standards development process. An appeals mechanism safeguards both those who are directly and or materially affected by the process and the standards developing organization.

9.1   Appeals related to ANSI/JEDEC standards and publications

The following appeals procedures shall be used for actions taken within the JEDEC standards process for the development of ANSI/JEDEC standards and publications.

9.1.1   Right of appeal

Persons who have directly and or materially affected interests and who have been or will be adversely affected by a standard or publication within ANSI jurisdiction have the right to appeal substantive or procedural actions or inactions of JEDEC formulating groups.

The burden of proof to show an adverse effect shall be on the appellant. Appeals shall be directed to the JEDEC Office in accordance with the appeals procedures as defined in this section.

JEDEC Manual No. 21T
Page 30

9.1.2   Criteria for appeals mechanism

The following general criteria are encompassed in these appeals procedures:

a) Appeals shall be addressed promptly and a decision made expeditiously;

b) The right of the involved parties to present their cases shall not be denied;

c) These procedures shall provide for participation by all parties concerned without imposing an undue burden on them;

d) Consideration of appeals shall be fair and unbiased and shall fully address the concerns expressed; and

e) Records of appeals shall be kept and made available upon request. The JEDEC Office may levy an appropriate charge to cover the cost of reproduction, handling, and distribution of materials. The fee shall be predetermined, fixed, and reasonable. A procedure for requesting a fee waiver or fee reduction shall be available.

9.1.3   Appeals procedures

The following subsections outline the JEDEC Appeals Procedures. In the case of an appeal to ANSI of a JEDEC action or inaction on an ANSI/JEDEC standard, the appellant may waive the right of the JEDEC appeals process, see 9.1.4.

9.1.3.1 Complaints

The appellant shall file a written complaint with the JEDEC Office within 30 calendar days after the date of the action being appealed or at any time with respect to inaction. The complaint shall state the nature of the objection(s) including any adverse effects, the section(s) of these procedures or the standard(s) that are at issue, action(s) or instances of inaction that are at issue, and the specific remedial action(s) that would satisfy the appellant's concerns. Previous efforts to resolve the objection(s) and the outcome of each shall be noted.

9.1.3.2 Response

Within 30 calendar days after receipt of the complaint, the respondent (formulating group chairman or JEDEC representative) shall respond in writing to the appellant, specifically addressing each allegation of fact in the complaint to the extent of the respondent's knowledge. Complaints that are technical in nature shall be referred to the appropriate JEDEC formulating committee having jurisdiction over the material for review and possible action. Complaints that are procedural in nature shall be referred to the JEDEC Board for review and possible action.

9.1.3.3 Hearing

If the appellant and the respondent are unable to resolve the written complaint informally in a manner consistent with these procedures within 15 calendar days, the JEDEC Office shall schedule a hearing with an appeals panel* on a date agreeable to all participants but within 30 calendar days, giving at least 10 calendar days' notice. Hearing on the complaint will take place at the next regular meeting of the JEDEC formulating committee or the JEDEC Board depending on the nature of the complaint.

NOTE   In the case of an ANSI appeal, see Annex D.10 for clarification of an appeals panel.

9.1.3.4 Conduct of the hearing

The appellant has the burden of demonstrating adverse effects, improper actions or inactions, and the efficacy of the requested remedial action.

9.1.3.5 Decision

The appeal disposition shall be documented by the formulating committee for technical matters and by the JEDEC Board for procedural matters. A record of the appeals shall be kept by JEDEC and made available to the involved parties.

NOTE   In the case of an ANSI appeal, the appeals panel shall render its decision in writing within 30 days of the hearing, based upon a preponderance of the evidence, stating its findings of fact and conclusions, with reasons therefore and citing the evidence. The Committee Secretary shall notify the appellant and the Committee of the decision of the appeals panel, which shall be binding and final on all concerned.

If, for whatever reason(s), the appellant chooses to forego the process detailed above, the JEDEC Office shall maintain all documents pertaining to JEDEC attempts to resolve the matter at hand. These documents may be used in any further appeals proceedings.

9.1.4   Further appeal

If the matter under appeal relates to a JEDEC Standard that has been or is expected to be recognized as an American National Standard, subsequent further appeal may be made directly to ANSI. If the appellant gives notice to the JEDEC Office that further appeal to ANSI is intended, a full record of the complaint, response and decision shall be submitted by the JEDEC Office to ANSI.

NOTE   ANSI will not normally hear an appeal of an action or inaction by JEDEC until the appeals process has been completed. Such appeals shall be directed to ANSI in accordance with the procedures of the appropriate ANSI entity (e.g., Board of Standards Review, Executive Standards Council, etc.).

9.2   Appeals not related to ANSI/JEDEC standards and publications

The following appeals procedures shall be used for actions taken within the JEDEC standards process that are not related to the development of ANSI/JEDEC standards and publications.

9.2.1   Right of appeal

Committee Members or Participants who have directly and or materially affected interests and who have been or will be adversely affected by the activities of another Committee Member or Representative, a JEDEC committee, or a JEDEC standard or publication have the right to appeal technical or procedural actions or inactions.

The burden of proof to show an adverse effect shall be on the appellant. Appeals shall be directed to the JEDEC Office in accordance with the appeals procedures as defined in this section.

JEDEC Manual No. 21T
Page 32

9.2.2   Criteria for appeals mechanism

The following general criteria are encompassed in these appeals procedures:

a) Appeals shall be addressed promptly and a decision made expeditiously;

b) The right of the involved parties to present their cases shall not be denied;

c) These procedures shall provide for participation by all parties concerned without imposing an undue burden on them;

d) Consideration of appeals shall be fair and unbiased and shall fully address the concerns expressed; and

e) Records of appeals shall be kept and made available upon request. The JEDEC Office may levy an appropriate charge to cover the cost of reproduction, handling, and distribution of materials.

9.2.3   Appeals procedures

The following subsections outline the JEDEC Appeals Procedures for appeals that are not related to ANSI/JEDEC standards and publications.

9.2.3.1 Complaints

The appellant shall file a written complaint with the JEDEC Office within 30 calendar days after the date of the action being appealed or at any time with respect to inaction. The complaint shall state the nature of the objection(s) including any adverse effects, the section(s) of these procedures or the Standard(s) that are at issue, action(s) or instances of inaction that are at issue, and the specific remedial action(s) that would satisfy the appellant's concerns. Previous efforts to resolve the objection(s) and the outcome of each shall be noted.

9.2.3.2 Response

Within 30 calendar days after receipt of the complaint, the respondent(s) shall respond in writing to the appellant, specifically addressing each allegation of fact in the complaint to the extent of the respondent's knowledge.

Complaints that are technical in nature shall be referred to the appropriate JEDEC committee having jurisdiction over the material for review and possible action. Complaints that are non-technical or procedural in nature shall be referred to the JEDEC Board for review and possible action. Complaints that relate to the patent policy shall be referred to the JEDEC Board for review and possible action.

9.2.3.3 Hearing

If the appellant and the respondent are unable to resolve the written complaint informally in a manner consistent with these procedures within 30 calendar days, the JEDEC Office shall schedule a hearing with an impartial appeals panel consisting of three individuals appointed by the committee or the JEDEC Board, as appropriate, on a date agreeable to all parties, giving at least 10 calendar days' notice. Hearing on the complaint will take place in person or by telephone.

9.2.3   Appeals procedures (cont'd)

9.2.3.4 Conduct of the hearing

The appellant has the burden of demonstrating adverse effects, improper actions or inactions, and the efficacy of the requested remedial action.

9.2.3.5 Decision

The appeal disposition shall be documented by the JEDEC appeals panel. A record of the appeals shall be kept by JEDEC and made available to the involved parties.

Appeal dispositions on complaints that are technical in nature may be further appealed to the appropriate JEDEC committee. Appeal dispositions on complaints that are non-technical or procedural in nature may be further appealed to the JEDEC Board of Directors.

10   External publicity

All articles, presentations, news releases, or other publicity must be approved by JEDEC Legal Counsel prior to release.

Articles, speeches, and other presentations for publication or delivery by members of the Board, its committees, or JEDEC staff that cover specific JEDEC work or JEDEC policy or purports to speak on behalf of JEDEC must be approved by the Board, if time permits; otherwise by the Board chairperson who shall be responsible for ensuring that the content is accurate and reflects current JEDEC policy. Any publicity that speaks for the Board shall require similar approval.

The committee chairperson may talk to the press and approve technical and tradeshow presentations about ongoing committee work when it is appropriate to promote a particular standard or the work of the committee. This public disclosure should be limited to the goal of the standard under development and any details of the standard that have been approved by committee ballot(s).

Companies may not advertise or give press releases stating that their products comply with a JEDEC standard, publication, or registration prior to Board approval of the documents.

JEDEC Manual No. 21T
Page 34

11   JEDEC ethics rules for electronic communications

No JEDEC member or alternate shall post to an e-mail reflector, bulletin board, or Web site owned or sponsored by JEDEC, any of the following:

a)   any advertising or marketing information,

b)   any cost or pricing information,

c)   any proprietary information,

d)   any non-JEDEC copyright information or material that is in excess of that allowed under current USA copyright laws,

e)   any technical information that requires a USA government export license before it is transferred outside of the United States,

f)   information covered by USA secrecy laws,

g)   solicitations, or requests for contributions to "for profit" or "non-profit" (charitable) organizations,

h)   chain letters,

i)   job search or hiring information,

j)   computer games or other software products,

k)   files with known software viruses,

l)   offensive material covering:
   1)   libel (i.e., false or malicious statements),
   2)   threats, retaliation, or intimidation,
   3)   use of language that is obscene or in poor taste, including jokes,
   4)   sexual harassment or inappropriate sexual content, such as pictures, images, messages, or cartoons,
   5)   discriminatory communication relating to race, color, national origin, sex, marital status, sexual orientation, age, veteran's status, disability, religious or political beliefs.

All electronic communications and posting must comply with this JEDEC Manual and the JEDEC Legal Guides.

Annex A (normative) Legal guidelines summary

A.1   JEDEC patent policy summary

• All JEDEC Member Companies and their Representatives agree to abide by the JEDEC patent policy.

• The commitment applies to all entities, including non-committee members, that have a Representative present at any point in a meeting of a JEDEC Committee or Task Group.

• The commitment continues as long as the Committee Member or Representative is a member of or a participant in a particular JEDEC Committee.

• For the purposes of the patent policy, "Committee" refers to the full committee, except for those committees that have subcommittees. In that context, "committee" refers to any group that has a separate scope.

• All companies and their representatives are required to disclose all known Potentially Essential Patent Claims owned or controlled by the company.

• No company has a duty to conduct a search for Potentially Essential Patent Claims.

• All companies, as a condition of committee membership or participation, agree to license their Essential Patent Claims on RAND terms and conditions.

• The licensing assurance must indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee, and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.

• If a Member Company knows it would be unwilling to license its Essential Patent Claims on RAND terms, the member must notify the committee chair and withdraw from the committee within 120 days after giving the notice. This option is not available to a Member Company with respect to its own Contribution.

• Companies and their representatives are required to use a standard form for the disclosures and assurances.

• The disclosure and licensing obligations of companies and their representatives are limited to Standards developed in the particular JEDEC committees in which they are members or in which they participate.

• The obligations apply to all entities, including non-committee members, that have a representative present at any point in a meeting of a JEDEC Committee or Task Group.

• Member Companies and their Representatives are strongly encouraged to review their current committee and subcommittee assignments, and ensure they are prepared to accept the commitments defined by the patent policy.

See, 8.2 for additional information.

A.2   Copyright material

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, it shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC Office, and the standard or publication shall include a reference to such permission as a footnote.

JEDEC Manual No. 21T
Page 36

A.3   License Assurance/Disclosure Form (See 8.2.3 and 8.2.5 of the JEDEC Patent Policy)

For the electronic version of the License Assurance/Disclosure Form go
to: http://www.jedec.org/sites/default/files/License_Assurance-Disclosure_Form_20150710.pdf

Part 1

Date: _____

Entity Name: _____

Address: _____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

Part 2

Identify the relevant JEDEC Standard:

_____

_____

Part 3

For Issued Patents:

Patent No: _____

Patent Name or Title: _____

Country of Issuance: _____

For Published Patent Applications:

Published Patent Application No. :_____

Patent Application Name or Title: _____

Country of Filing: _____

For Unpublished Patent Applications:

Subject Matter of Patent Application:

_____

_____

A.3   License Assurance/Disclosure Form (cont'd)

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

Part 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

___ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

___ (ii) A license will be offered, with compensation, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

Such assurance shall indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee[8], and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.

The assurance shall also indicate that it is intended to be binding on successors-in-interest regardless of whether such provisions are included in the relevant transfer documents.

---

[8] Committee Members and Representatives may comply with (i) and (ii) by notifying the transferee in writing that the RAND licensing obligations under Section 8.2.4 of the JEDEC Patent Policy are binding on the Committee Member or Representative, the transferee and subsequent transferees or a general statement in the transfer or assignment agreement that the Patent Claim(s) being transferred or assigned are subject to any encumbrances, e.g., a RAND licensing obligation, that may exist as of the effective date of such agreement.

JEDEC Manual No. 21T
Page 38

A.3   License Assurance/Disclosure Form (cont'd)

Part 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

_____
(Signature)
_____
(Name printed)
_____
(Date)

NOTE   *The committee or task group has the right to request additional technical information relating to the Patent*
or Patent Application in order to consider workarounds and other technical alternatives.

RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG

A.4   Notice of Refusal to Offer Licenses on RAND Terms

Part 1

Date: _____

Committee Member: _____

Entity Mailing Address: _____

IPR Contact Name: _____

IPR Contact Telephone Number: _____

IPR Contact E-Mail Address: _____

Part 2

Identify the relevant JEDEC Standard:

_____

Part 3

Pursuant to 8.2.3.1 of the JEDEC Patent Policy, the Committee Member hereby provides notice that the Committee Member is not willing to offer a license on RAND terms to the Potentially Essential Patents identified in A.4, Part 4.

Part 4

For Issued Patents (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. Patent Name or Title: _____
3. Patent Number: _____
4. Country of Issuance: _____
5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:

    _____

For Published Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. Published Patent Application Number: _____
3. Patent Application Name or Title: _____
4. Country of Filing: _____
5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:

    _____

JEDEC Manual No. 21T
Page 40

A.4   Notice of Refusal to Offer Licenses on RAND Terms (cont'd)

For Unpublished Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. General Subject Matter of Patent Application: _____

_____

3. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:

_____

Part 5

By signing this Notice, the IPR Contact represents that they are authorized to complete and submit this Notice on behalf of the Committee Member. Pursuant to Section 8.2.3.1 of the JEDEC Patent Policy, the IPR Representative represents that the information provided in this Notice does not include a contribution that was contributed by the Committee Member. If the Committee Member becomes aware of any other Potentially Essential Patent not already covered by a Notice and the ballot period is open, then the Committee Member may submit additional Notices.

_____
Signature of IPR Contact

Accepted and Agreed to:

_____
JEDEC

_____

Date Accepted: _____

RETURN THE COMPLETED NOTICE BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG

Annex B (informative) Patent policy application guidelines

The following points describe the application of the JEDEC patent policy:

B.1   Committee discussion of pending or existing patents is a permissible activity and is encouraged when the committee feels that the patented item or process represents the best technical basis for a standard.

B.2   Discussion of a pending or existing patent does not constitute an acknowledgment of the validity of the patent, because validity is based on prior art and determination of the company/individual that first made the invention or applied for the patent. The committee's concern is only with the technical merits of the patent and whether the technical proposal is a sound basis for standardization.

B.3   By its terms, the JEDEC patent policy applies with equal force to situations involving:

    a)   the discovery of patents that may be required for use of a standard subsequent to its adoption, and

    b)   the initial issuance of a patent after the adoption of a standard.

Once disclosure is made, the holder is obligated to provide the same assurances to JEDEC as are required in situations where patents exist or are known prior to approval of a proposed standard.

Thus, if notice is given of a patent that may be required for use of an already approved JEDEC standard, a standards developer may wish to make it clear to other standards-making participants that the JEDEC procedures require the patent holder to provide the assurances contained in the patent policy or suffer the withdrawal of JEDEC's approval of the document as a JEDEC standard.

JEDEC Manual No. 21T
Page 42

Annex C (normative) ANSI Standardization Procedures

For those documents that are intended for publication as an American National Standard (ANS), the provisions set forth in this annex apply.

C.1   Notification of American National Standards (ANS) development

Notification of American National Standards activity shall be announced in suitable media as appropriate to demonstrate provision of opportunity for participation by all directly and materially affected persons. At the initiation of a project to develop or revise a Standard, notification shall be transmitted to ANSI using the Project Initiation Notification System (PINS) form, or its equivalent, for listing in Standards Action. A PINS form may be submitted, but is not required, at the initiation of a project to reaffirm or withdraw a Standard. Prompt consideration shall be given to the written views and objections of all participants, including those commenting on the PINS announcement. Comments resulting from the filing of PINS will be handled in accordance with the ANSI Essential Requirements, 2.5.

C.2   Submission to ANSI for public review

Following approval of the standard, responsible JEDEC Standards staff shall submit the proposed ANS to ANSI to initiate public review. JEDEC Standards staff shall provide appropriate documentation to ANSI. Responsible JEDEC Standards staff shall receive, collect and acknowledge receipt of public review comments. In addition, responsible JEDEC Standards staff shall forward all public review comments to the formulating group for review and response. The response to each commenter shall include a notation of the JEDEC and ANSI appeals process.

NOTE   A proposed ANS is subject to comment only (not for vote) during public review and by any and all materially or directly affected parties.

C.3   Public review comments

JEDEC Standards staff shall acknowledge receipt of a public review comment, regardless of its nature. The only comments normally addressed by a working group or formulating group are editorial or technical in nature. Technical comments should be accompanied with wording that would aid the formulating group in addressing the comments.

Other comments may be handled in the following manner on behalf of the formulating group:

- The JEDEC Legal Counsel shall respond to comments relating to legal concerns;

- JEDEC Standards staff shall respond to comments relating to concerns regarding the standards development process;

- The formulating group with input from JEDEC staff shall address scope concerns;

- The reason for non-acceptance shall be sent regarding editorial or technical concerns;

- Vague comments shall be returned to the respondent requesting expeditious clarification.

JEDEC Standards staff shall retain copies of response to comments.

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.4   Public review commenter response

The commenter shall have 14 calendar days after response to acknowledge the acceptance or rejection of that reply. If no response is received, the responsible JEDEC Standards staff shall send a reminder notice to the commenter requesting response. If no response is received within an additional 5 calendar days, the responsible JEDEC Standards staff will send a registered letter to the commenter noting the lack of response. The commenter's comments are then recorded as unresolved and circulated to the formulating group per the provisions of C.3.

All correspondence showing the formulating group's effort to address the comments, noting a lack of response when appropriate, shall be included in any package of materials provided to ANSI.

C.5   Results scenarios

Results scenario #1: If no comments are received after the close of public review, the document shall be forwarded to ANSI with a request for approval.

Results scenario #2: If editorial comments are received by the close of public review, the document editor, editing group, or chair shall address the comments. The document, with edits, if any, shall be forwarded to ANSI for approval.

Results scenario #3: If substantive comments are received from public review, the working group or formulating group shall review these comments, and attempt to resolve them, and notify each commenter of said action (see C.4), along with a notification of the JEDEC and ANSI appeals process.

a)   If no substantive changes are made, the document is forwarded to ANSI for approval.

b)   If substantive changes are made, the formulating group shall conduct a recirculation vote/ballot and "second" public review (see C.4).

c)   If negative, substantive comments remain unresolved from public review, the formulating group shall conduct a recirculation vote/ballot, and, if necessary, a "second" public review (see C.4).

JEDEC Manual No. 21T
Page 44

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.6   Voting on an American National Standard

When a vote in a formulating group is for the purpose of approving a document for publication as an American National Standard, a Ballot Summary (Tally of votes) shall be prepared and included in the minutes. The Interest Category is normally self-selected by the voting member.

Action Required	Method (all calendar days)	Approval Criteria
Meeting Vote*	At the meeting	Two-thirds voting
Ballot	30 day ballot	Two-thirds voting
ANSI BSR8 (Public review)	Initial 60 day comment period [30 or 60 day subsequent comment period(s)] (or other ANSI designated time period where applicable)	Comments addressed by formulating group

* Voting members not present at the time of the vote shall be given the opportunity to vote on the standard after the meeting. The JEDEC staff shall notify the absent voting members via e-mail of any substantive changes made to the standard subsequent to the 21 day ballot period and advise that they have 7 days to cast their vote via the JEDEC Voting Machine. Any absent voting members that fail to respond shall be listed as No Response on the final submittal for approval to ANSI. Response to this opportunity to vote shall not be considered as attendance at the meeting for purposes of voting maintenance.

C.7   Legal approval

All ANSI/JEDEC standards shall receive JEDEC legal approval before publication.

C.8   ANSI approval

If ANSI/BSR is approved, responsible JEDEC Standards staff is notified and in turn publishes the document.

If ANSI/BSR does not approve, comment resolution issues will be dealt with by the formulating group and process-related issues will be dealt with by JEDEC Standards staff. If the ANSI/BSR comments are resolved and the document is approved, responsible JEDEC Standards staff publishes the document.

If the comments cannot be resolved, the document is returned to the formulating group for further resolution or cancellation. The formulating group may appeal the actions of the ANSI/BSR.

C.9   ANSI patent policy

If a JEDEC standard is intended for an American National Standard, then the standard must comply with the current ANSI patent policy.

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.10   Appeals panel (for an appeal of an ANS)

In the case of an ANSI appeal, the appeals panel shall consist of three individuals who have not been directly involved in the matter in dispute, and who (knowingly in good faith) will not be materially or directly affected by any decision made or to be made in the dispute. At least two members shall be acceptable to the appellant and at least two members shall be acceptable to JEDEC. In the event the appellant does not wish to select a panelist or a third panelist cannot be agreed upon, JEDEC shall appoint this individual to the panel in order to hold a hearing.

C.11   ANSI Commercial Terms and Conditions

Provisions involving business relations between buyer and seller such as guarantees, warranties, and other commercial terms and conditions shall not be included in an ANS.

JEDEC Manual No. 21T
Page 46

Annex D (informative) Differences between revisions

This annex briefly describes most of the changes made to entries that appear in this standard, JM21T, compared to its predecessor, JM21S (November 2015). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of Change
1.4.4	4), Removed "within a calendar year" from 1st sentence, removed "Participation via teleconference is allowed only once per calendar year" and replaced with ". It is the expectation that Directors attend all Board meetings, at minimum Directors must attend at least one face-to-face Board meeting, in person, each calendar year." (JCB-19-27)
3.5	Quorum: Changed "20" to "12". (JCB-19-04)
1.4.3.3	Changed to 1.4.3.4. (JCB-20-14)
1.4.3.3	New subclause added. (JCB-20-14)
8.2.1	New term and definition added for "Approval by the Committee". (JCB-20-15)
8.2.2.2	4th paragraph, last sentence, modified as follows: The sole remedy for any issues or concerns about deviations from approved scope shall be an appeal to the JEDEC Board of Directors made prior to approval of the subject draft specification for resolution Approval by the Committee, see 9.2. (JCB-20-15)
8.2.3	4th paragraph, last sentence, modified as follows: Such disclosures or notices of known Potentially Essential Patents shall be delivered to the JEDEC Legal Department within thirty (30) calendar days of draft specification completion Approval by the Committee in order to be effective. (JCB-20-15)
8.2.3.1	1st paragraph, modified as follows: … reasonably possible but no later than thirty (30) calendar days after completion of the draft specification Approval by the Committee in the form of a Notice of Refusal to offer Licenses on RAND Terms, see Annex A.4. (JCB-20-15)

D.1   Differences between JM21S and JM21R (July 2015)

Clause	Description of Change
3.4	2nd para., 1st sentence modified as follows: A JEDEC staff member or a designated alternate must be in attendance at participate in every committee meeting, either in person or by electronic means.

EXHIBIT H

**RETURN THE COMPLETED FORM BY MAIL TO JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107 OR BY E-MAIL TO
JOHNK@JEDEC.ORG**

License Assurance/Disclosure Form

PART 1

Date: April 7, 2016

Entity Name: Netlist, Inc.

Address: 175 Technology, #150

Irvine, CA 92618

IPR Contact: Noel Whitley, VP of Intellectual Property

Phone: 949-679-0115

E-Mail: nwhitley@netlist.com

PART 2

Identify the relevant JEDEC Standard(s):

JC40-DDR4 LRDIMM components (RCD&DB) protocol and functionality module;

JC42-DDR4 High Bandwidth Memory DRAM; JC45-DDR4 LRDIMM

PART 3

For Issued Patents:

Patent No.: 8001434

Patent Name or Title: Memory board with self-testing capability

Country of Issuance: US

For Published Patent Applications:

Published Patent Application No.:

Patent Application Name or Title:

Country of Filing:

For Unpublished Patent Applications:

Subject Matter of Patent Application:

(See JM21, 8.2.3 and 8.2.5 of the JEDEC Patent Policy for additional details.)

License Assurance/Disclosure Form

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

PART 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

_____   (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

✓   (ii) A license will be offered to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

Such assurance shall indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee[1], and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.

The assurance shall also indicate that it is intended to be binding on successors-in-interest regardless of whether such provisions are included in the relevant transfer documents.

PART 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

IPR Contact: _____

Phone: _____   E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

_____   April 7, 2016
(Signature)   (Date)
Noel Whitley, VP of Intellectual Property
(Name printed)

NOTE   The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

---

[1] Committee Members and Representatives may comply with (i) and (ii) by notifying the transferee in writing that the RAND licensing obligations under Section 8.2.4 of the JEDEC Patent Policy are binding on the Committee Member or Representative, the transferee and subsequent transferees or a general statement in the transfer or assignment agreement that the Patent Claim(s) being transferred or assigned are subject to any encumbrances, e.g., a RAND licensing obligation, that may exist as of the effective date of such agreement.

EXHIBIT I

RETURN THE COMPLETED FORM BY MAIL TO JEDEC, ATTENTION: LEGAL DEPARTMENT, 3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107 OR BY E-MAIL TO JOHNK@JEDEC.ORG

License Assurance/Disclosure Form

PART 1

Date: April 7, 2016

Entity Name: Netlist, Inc.

Address: 175 Technology, #150

Irvine, CA 92618

IPR Contact: Noel Whitley, VP of Intellectual Property

Phone: 949-679-0115

E-Mail: nwhitley@netlist.com

PART 2

Identify the relevant JEDEC Standard(s):

JC40-DDR4 LRDIMM components (RCD&DB) protocol and functionality module, DDR4 RDIMM RCD; JC45-DDR4 LRDIMM, DDR4 RDIMM

PART 3

For Issued Patents:

Patent No.: 8489837

Patent Name or Title: Systems and methods for handshaking with a memory module

Country of Issuance: US

For Published Patent Applications:

Published Patent Application No.:

Patent Application Name or Title:

Country of Filing:

For Unpublished Patent Applications:

Subject Matter of Patent Application:

(See JM21, 8.2.3 and 8.2.5 of the JEDEC Patent Policy for additional details.)

License Assurance/Disclosure Form

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

PART 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

_____ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

✓ (ii) A license will be offered to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

Such assurance shall indicate that the patent holder (or third party authorized to make assurances on its behalf) will include in any documents transferring ownership of patents subject to the assurance, provisions sufficient to ensure (i) that the commitments in the assurance are binding on the transferee[1], and (ii) that the transferee will similarly include appropriate provisions in the event of future transfers with the goal of binding each successor-in-interest.

The assurance shall also indicate that it is intended to be binding on successors-in-interest regardless of whether such provisions are included in the relevant transfer documents.

PART 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

IPR Contact: _____

Phone: _____   E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

_____   April 7, 2016
(Signature)   (Date)
Noel Whitley, VP of Intellectual Property
(Name printed)

NOTE   The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

---

[1] Committee Members and Representatives may comply with (i) and (ii) by notifying the transferee in writing that the RAND licensing obligations under Section 8.2.4 of the JEDEC Patent Policy are binding on the Committee Member or Representative, the transferee and subsequent transferees or a general statement in the transfer or assignment agreement that the Patent Claim(s) being transferred or assigned are subject to any encumbrances, e.g., a RAND licensing obligation, that may exist as of the effective date of such agreement.

EXHIBIT J

N E T L I S T

<u>VIA U.S. MAIL & ELECTRONIC MAIL</u>

April 1st, 2010

Mr. John Kelly
President, JEDEC
3103 North 10th Street
Suite 240-S
Arlington, Virginia 22201

Re: <u>Netlist, Inc. Patents and Patent Applications That Are Potentially Relevant to JC 40
      and JC 42</u>

Dear Mr. Kelly:

As you are aware, in 2007 Netlist informed JEDEC that Netlist has intellectual property
that may cover certain implementations of the Advanced Memory Buffer Quad Rank
Support Standard ("the Standard") and that we would RAND all such intellectual
property. In January 2008, Netlist submitted a RAND letter to JEDEC for U.S. Patent
No. 7,289,386, indicating we will license the patent to applicants for purposes of
implementing the Standard with compensation on reasonable terms and conditions that
are demonstrably free of discrimination.

A continuation of the '386 Patent, U.S. Patent No. 7,619,912 (the "'912 Patent"), issued in
November 2009, and it has come to Netlist's attention that questions have been raised as
to whether the '912 Patent falls within the scope of Netlist's original statement that the
letter would RAND Netlist intellectual property that may cover the Standard. Netlist
submits this letter to clarify its position on the matter and states that--consistent with its
original statement in 2007-- Netlist is willing to license the '912 Patent to applicants for
purposes of implementing the Standard with compensation on reasonable terms and
conditions that are demonstrably free of discrimination.

Sincerely,

Mario J. Martinez
JEDEC Representative
Netlist, Inc.

EXHIBIT K

License Assurance/Disclosure Form

PART 1

Date: _11/22/10_

Entity Name: _Netlist, Inc._

Address: _51 Discovery, Suite 150_
Irvine, CA 92618

IPR Contact: _Mario Martinez_

Phone: _949 679 0159_

E-Mail: _mmartinez@netlist.com_

PART 2

Identify the relevant JEDEC Standard:

_JC42.3   3DS   (#1655.19, #1644.96, #1655.1)_

JC45   LRDIMM (#2192.62, #2192.43, #2192.58, #2192.57)

PART 3

For Issued Patents:

Patent No.: _7,519,912_

Patent Name or Title: _Memory Module Decoder_

Country of Issuance: _United States_

For Published Patent Applications:

Published Patent Application No.: _____

Patent Application Name or Title: _____

Country of Filing: _____

For Unpublished Patent Applications:

Subject Matter of Patent Application:

_____

_____

(See JM21P, 8.2.3 and 8.2.5 of the JEDEC Patent Policy for additional details)

51

License Assurance/Disclosure Form

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

PART 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

___ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

✓ (ii) A license will be offered to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

PART 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

_____   _____ 11/30/2010 _____
(Signature)   (Date)

_____ MARIO MARTINEZ _____
(Name printed)

NOTE: The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

**RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG**

6/

EXHIBIT L

Notice of Refusal to Offer Licenses on RAND Terms Form

PART 1

Date: December 6th, 2010

Committee member: Mario Martinez

Mailing Address: 51 Discovery

Irvine, CA 92618

IPR Contact: Mario Martinez

Phone: 949-679-0159

E-Mail: mmartinez@netlist.com

PART 2

Identify the relevant JEDEC Standard:
JC40 - Item 142.55A Memory Buffer Spec Electrical, Item 142.43 Memory Buffer MemBist,

JC40 - Item 142.50a Memory Buffer Spec Reset

PART 3

Pursuant to JM21P, 8.2.3.1 of the JEDEC Patent Policy, the Committee Member hereby provides notice that the Committee Member is not willing to offer a license on RAND terms to the Potentially Essential Patents identified in JM21P, Annex A.4, Part 4.

PART 4

For Issued Patents (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. Patent Name or Title: _____ Memory Module Decoder
3. Patent Number: _____ 7,619,912
4. Country of Filing: United States
5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information

(See JM21P, 8.2.3 and 8.2.5 of the JEDEC Patent Policy for additional details)

5

Notice of Refusal to Offer Licenses on RAND Terms Form

For Published Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____

2. Published Patent Application Number: _____

3. Patent Application Name or Title: _____

4. Country of Filing: _____

5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information

_____

For Unpublished Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____

2. General Subject Matter of Patent Application:

_____

_____

3. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information

_____

PART 5

By signing this Notice, the IPR Contact represents that they are authorized to complete and submit this Notice on behalf of the Committee Member. Pursuant to JM21P, 8.2.3.1 of the JEDEC Patent Policy, the IPR Representative represents that the information provided in this Notice does not include a contribution that was contributed by the Committee Member. If the Committee Member becomes aware of any other Potentially Essential Patent not already covered by a Notice and the ballot period is open, then the Committee Member may submit additional Notices.

_____
Signature of IPR Contact

Accepted and Agreed to:

_____   _____
JEDEC   Date Accepted

RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG

EXHIBIT M

License Assurance/Disclosure Form

PART 1

Date: _9/7/11_

Entity Name: _Netlist, Inc._

Address: _51 Discovery, Suite 150_

Irvine, CA 92618

IPR Contact: _Jayesh Bhakta_

Phone: _949 435 0025_

E-Mail: _jbhakta@netlist.com_

PART 2

Identify the relevant JEDEC Standard:

_JC40_

PART 3

For Issued Patents:

Patent No.: _7,519,912_

Patent Name or Title: _Memory Module Decoder_

Country of Issuance: _USA_

For Published Patent Applications:

Published Patent Application No.: _____

Patent Application Name or Title: _____

Country of Filing: _____

For Unpublished Patent Applications:

Subject Matter of Patent Application:

_____

_____

(See JM21P, 8.2.3 and 8.2.5 of the JEDEC Patent Policy for additional details)

License Assurance/Disclosure Form

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

PART 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

☐ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

☑ (ii) A license will be offered to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

PART 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

Jayjash Bharath   _9/7/2011_
(Signature)   (Date)

Cheif Module Architect.
(Name printed)

NOTE: The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

**RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG**

EXHIBIT N

JEDEC
STANDARD

Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3 RDIMM Applications

JESD82-29

DECEMBER 2009

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Exhibit 63

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

PRICE: Contact JEDEC

Exhibit 63

Exhibit 63

Exhibit 63

DEFINITION OF THE SSTE32882 REGISTERING CLOCK DRIVER WITH PARITY AND QUAD CHIP SELECTS FOR DDR3 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-09-40, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

---

1   Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTE32882 registered buffer with parity for driving address and control nets on DDR3 RDIMM applications.

The purpose is to provide a standard for the SSTE32882 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE   The designation SSTE32882 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

---

2   Device standard

2.1   Description

This 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for 1.5V or 1.35V V_{DD} operation.

All inputs are 1.5/1.35V CMOS compatible. All outputs are 1.5/1.35V CMOS drivers optimized to drive single terminated 25..50 Ohms traces in DDR3 RDIMM applications. The clock outputs Yn and Yn# and control net outputs QnCKEn, QnCSn# and QnODTn can be driven with a different strength and skew to compensate for different loading and equalize signal travel speed.

The SSTE32882 has two basic modes of operation associated with the Quad Chip Select Enable (QCSEN#) input. When the QCSEN# input pin is open (or pulled HIGH), the component has two chip select inputs, DCS0# and DCS1#, and two copies of each chip select output, QACS0#, QACS1#, QBCS0# and QBCS1#. This is the "QuadCS disabled" mode. When the QCSEN# input pin is pulled LOW, the component has four chip select inputs DCS[3:0]#, and four chip select outputs, QCS[3:0]#. This is the "QuadCS enabled" mode. Through the remainder of this specification, DCS[n:0]# will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. QxCS[n:0]# will indicate all of the chip select outputs.

The SSTE32882 operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going HIGH, and CK# going LOW. The data could be either re-driven to the outputs once exactly one of the input signals DCS[n:0]# is driven LOW or it could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in 2.2.

Based on control register settings the device can change its output characteristics to match different DIMM net topologies. The timing can be changed to compensate for different flight time of signals within the target application. By disabling unused outputs the power consumption is reduced.

Exhibit 63

JEDEC Standard No. 82-29
Page 2

2.1 Description (cont'd)

2.1.1 Initialization

The LV (Low Voltage) SSTE32882 can be powered-on at 1.5V or 1.35V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET# asserted. When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. Therefore the reference voltage (V_{REF}) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE0, QACKE1, QBCKE0 and QBCKE1 must drive LOW during reset. All other outputs must float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW. After reset and after the stabilization time (t_{STAB}) the register must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3 RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two.

Figure 1 — Timing of clock and data during initialization sequence

(1) CK# is left out for better visibility

(2) DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range

(3) QxCKEn, QxODTn, QxCSn# are not included in this range.

(4) n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode

Exhibit 63

2.1   Description (cont'd)

2.1.1   Initialization (cont'd)

From a device perspective, the initialization sequence must be as shown in Table 1.

Table 1 — SSTE32882 Device Initialization Sequence[1]

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device						
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:0]²	DODT [0:1]	DCKE [0:1]	DA/C	PAR_IN	CK CK#	QCS# [n:0]²	QODT [0:1]	QCKE [0:1]	QxA/C	ERR OUT#	Y[0:3] Y#[0:3]	FB OUT³
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z	Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2⁴	V_{DD} 1.5V-->1.35V 1.35V-->1.5V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L⁵	Z	H⁵	Z	Z
3	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
4	V_{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L⁶	L	X	H	running	running
7⁷	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).						

1. X = Logic LOW or logic HIGH. Z = floating.
2. n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode
3. The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.
4. The system may power up using either 1.5V or 1.35V. The BIOS reads the SPD and adjusts the voltage if needed from 1.35V to 1.5V or from 1.5V to 1.35V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET# asserted.
5. QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5V or 1.35V (nominal).
6. This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}) us, the state of QxODTx is a function of DODTx (HIGH or LOW).
7. Step 7 is a typical usage example and is not a register requirement.

As part of the initialization all control words are reset to their default state which is "0", except for RC6 and RC7, which are vendor-defined. After initialization, the memory controller does only need to write to those control registers whose contents need to be changed.

2.1.1.1 Reset Initialization with Stable Power

The timing diagram in Figure 1 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# will be asserted for minimum 100ns. This RESET# timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3 Specification.

Exhibit 63

JEDEC Standard No. 82-29

Page 4

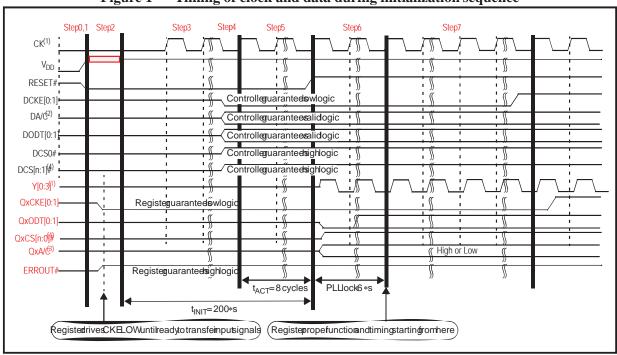## 2.1   Description (cont'd)

Figure 2 — Timing of clock and data during initialization sequence with stable power

[1] CK# left out for better visibility

[2] DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range

[3] QxCKEn, QxODTn, QxCSn# are not included in this range.

[4] n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.

Exhibit 63

2.1 Description (cont'd)

.

Table 2 — SSTE32882 Device Initialization Sequence[1] when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller							Outputs: Signals provided by the device						
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:1][2]	DODT [0:1]	DCKE [0:1]	DA/C	PAR_IN	CK CK#	QCS# [0:1]	QODT [0:1]	QCKE [0:1]	QxA/C	ERR OUT#	Y[0:3] Y#[0:3]	FB OUT[3]
0	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
1	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
2	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L[4]	Z	H[4]	Z	Z
3	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z	Z
4	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[5]	L	X	H	running	running
7	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).						

1. X = Logic LOW or logic HIGH. Z = floating.
2. n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode
3. The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.
4. QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and V_{DD} is nominal.
5. This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}) us, the state of QxODTx is a function of DODTx (HIGH or LOW).

2.1.2 Parity

The SSTE32882 includes a parity checking function. The SSTE32882 accepts a parity bit from the memory controller at its input pin PAR_IN one cycle after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain ERROUT# pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]# signals being LOW.

If an error occurs, and ERROUT# is driven LOW with the third input clock edge after the corresponding data on the D-inputs. It becomes high impedance with the 5th input clock cycle after the data corresponding with a parity error. In case of consecutive errors ERROUT# becomes high impedance with the 5th input clock cycle after the last data corresponding with a parity error. The DIMM-dependent signals (DCKE0, DCKE1, DCS0#, DCS1#, DODT0 and DODT1) are not included in the parity check computations.

2.1.2.1 Parity Timing Scheme Waveforms

The PAR_IN signal arrives one input clock cycle after the corresponding data input signals. ERROUT# is generated three input clock cycles after the corresponding data is registered. If ERROUT# goes LOW, it stays LOW for a minimum of two input clock cycles or until RESET# is driven LOW. Figure 3 shows the parity diagram with single parity-error occurrence and assumes the occurrence of only one parity error when data is clocked in at the n input clock cycle (PAR_IN clocked in on the n+1 input clock cycle).

Exhibit 63

JEDEC Standard No. 82-29
Page 6

2.1   Description (cont'd)

Figure 3 — Timing of clock, data and parity signals

(1) CK# left out for better visibility

Figure 4 shows the parity diagram with two consecutive parity-error occurrences and assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles).
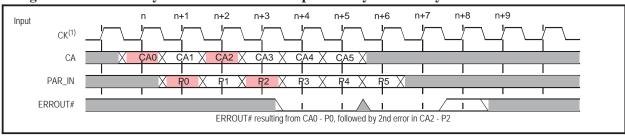
Figure 4 — Two Consecutive Parity-Error Occurrences

(1) CK# left out for better visibility

Figure 5 shows the parity diagram with two parity-error occurrences separated by a clock cycle with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+2 input clock cycles (PAR_IN clocked in on the n+1 and n+3 input clock cycles).

Figure 5 — Two Parity-Error Occurrences Separated by a Clock Cycle of no Error Occurrence

(1) CK# left out for better visibility

Figure 6 shows the parity diagram with two parity-error occurrences separated by two input clock cycles with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles).

Exhibit 63

2.1   Description (cont'd)

Figure 6 — Two Parity-Error Occurrences Separated by two Clock Cycle of no Error Occurrence

(1) CK# left out for better visibility

Figure 7 shows the parity diagram with two parity-error occurrences; during chip-select and chip-deselect modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles). Parity error in the chip-select mode is detected, but parity error in the chip-deselect mode is ignored.

Figure 7 — Parity-Error Occurrence In Chip-Deselect Mode

(1) CK# left out for better visibility

Figure 8 shows the parity diagram with two parity-error occurrences; during normal operation and during control register programming. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles). The data on the n+3 input clock pulse is intended for the control mode register. Parity error during control mode register programming is detected and the parity functionality is the same as during normal operation. If a parity error occurs, the command is ignored.

Figure 8 — Parity-Error Occurrences During Control Word Programming

(1) CK# left out for better visibility

Exhibit 63

JEDEC Standard No. 82-29
Page 8

2.1 Description (cont'd)

2.1.3 Power saving modes

The device supports different power saving mechanisms.

When both inputs CK and CK# are being held LOW the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1 which are kept driven LOW. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW for a certain period of time (t_{ACT}). The input clock must be stable for a time (t_{STAB}) before any access to the device takes place. Stopping the clocks (CK=CK#=LOW) will only put the SSTE32882 in the low-power mode and will not clear the content of the Control Words. The command mode registers will reset only when RESET# is driven LOW.

A float feature can be enabled by setting the corresponding bit in the control register. This causes the device to monitor all the DCS[n:0]# inputs and to float all outputs corresponding with the chip select gated inputs when all the DCS[n:0]# inputs are HIGH. If any one of the DCS[n:0]# input is LOW, the Qn outputs will function normally.

Once all the DCS[n:0]# inputs are HIGH, the gated address command inputs to the register can float to conserve input termination power. DCKE0, DCKE1, DODT0 and DODT1 need to be driven by the system all the time.

The RESET# input has priority over all other power saving mechanisms. When RESET# is driven LOW, it will force the Qn outputs to float, the ERROUT# output HIGH, the QACKE0, QACKE1, QBCKE0 and QBCKE1 outputs LOW and disables Input Bus Termination (IBT).

2.1.4 Register CKE Power Down

The SSTE32882 monitors both DCKEn input signals and enters into power saving state when it latches LOW on both DCKEn inputs and at least one of the DCKEn input has transitioned from HIGH to LOW. If either input Chip Select signal, DCS[n:0]#, is asserted together with DCKEn, the SSTE32882 transfers the corresponding command to its outputs together with QxCKEn LOW.

There are two modes of CKE Power Down selected by control word RC9. Bit DBA0 in RC9 indicates whether register turns off IBT or keeps IBT on.

2.1.4.1 Register CKE Power Down with IBT Off

Upon entry into CKE Power Down mode with IBT off, all register input buffers including IBT are disabled except for CK/CK#, DCKEn, FBIN, FBIN# and RESET#. The SSTE32882 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK/CK#, DCKEn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxODTn and QxCKEn outputs are driven LOW. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 9.

Exhibit 63

2.1 Description (cont'd)

Figure 9 — Power Down Mode Entry and Exit with IBT Off

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SSTE32882 into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn input are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the register immediately starts driving HIGH on the appropriate QxCKEn signal. The QxCSn# signals are driven HIGH and QxODTn signals are driven LOW. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all register outputs when QxCKEn goes HIGH. The register drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The register guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 9.

Exhibit 63

JEDEC Standard No. 82-29
Page 10

2.1   Description (cont'd)

2.1.4.2 Register CKE Power Down with IBT On

Upon entry into CKE Power Down Mode with IBT on, all register input buffers excluding IBT are disabled except for CK/CK#, DCKEn, DODTn, FBIN, FBIN# and RESET#. The SSTE32882 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK/CK#, DCKEn, DODTn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxCKEn outputs are driven LOW. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 10.

Figure 10 — Power Down Mode Entry and Exit with IBT On

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SSTE32882 into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

Exhibit 63

2.1   Description (cont'd)

To re-enable the SSTE32882 from this Power Down Mode with IBT on, valid logic levels are required at all device inputs when either or both DCKEn inputs are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the SSTE32882 immediately starts driving HIGH on the appropriate QxCKEn signals. The QxCSn# signals are driven HIGH and the QxODTn signals follow the inputs. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEn goes HIGH. The device drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 10.

2.1.5   Clock Stopped Power Down Mode

To support S3 Power Management mode or any other operation that allows Yn clocks to float, the SSTE32882 supports a Clock Stopped power down mode. When both inputs CK and CK# are being held LOW ($V_{IL\ (static)}$) or float (will eventually settle at LOW because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirement are shown in Figure 11, "Clock Stopped Power Down Entry and Exit with IBT On" and Figure 12, "Clock Stopped Power Down Entry and Exit with IBT Off". The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1, which must be kept driven LOW. The Clock Stopped power down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all register outputs besides QxCKE0 and QxCKE1 can be disabled.

Clock Stopped Power Down Mode Entry

To enter Clock Stopped Power Down mode, the register will first enter CKE power down mode. Once in CKE power down mode, DCKEn will continue be deasserted for a minimum of one tCKoff before pulling CK and CK# LOW. After holding CK and CK# LOW ($V_{IL\ (static)}$) for at least one tCKEV, both CK and CK# can be floated (because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer, CK/CK# will stay at LOW even though they are not being driven). The register is now in Clock Stopped Power Down mode. After CK and CK# are pulled LOW, DCKEn will remain LOW for at least one tCKEV before it can floated (if needed to be float). At this point, all input receivers and input termination of the SSTE32882 are disabled. The only active input circuits are CK and CK#, which are required to detect the wake up request from the host.

Clock Stopped Power Down Mode Exit

To wake up the register after entering Clock Stopped Power Down, the register inputs DCS[n:0]# must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, a frequency and phase accurate input clock signal must be applied. Within tACT after CK and CK# resumed normal operation, the SSTE32882 outputs start becoming a function of their corresponding inputs. The state of the DCS[n:0]# inputs must not be changed before the end of tSTAB. The input clock CK and CK# must be stable for a time equal or greater than tSTAB before any access to the SSTE32882 can take place.

Exhibit 63

JEDEC Standard No. 82-29
Page 12

2.1 Description (cont'd)

Figure 11 — Clock Stopped Power Down Entry and Exit with IBT On

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3

(2) With RC9 DBA0='0'

(3) When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.

(4) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

Exhibit 63

2.1 Description (cont'd)

Figure 12 — Clock Stopped Power Down Entry and Exit with IBT Off

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) With RC9 DBA0='1'
(3) When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.
(4) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

Exhibit 63

2.1   Description (cont'd)

2.1.6   Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling

Output Inversion is always enabled by default, after RESET# is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs, however the following B-outputs will be driven to the complement of the matching A-outputs: QBA3 - QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2.

Figure 13 — Output Inversion Functional Diagram

The Output Inversion feature is not used during DRAM MRS command access. When Output Inversion is disabled, all corresponding A and B output drivers of the SSTE32882 are driven to the same logic levels. Output Inversion must be disabled when the MRS and EMRS commands must be issued to the DRAMs, for example, to assure that the same programming is issued to all DRAMs in a rank.

With Output Inversion disabled during MRS access, in order to allow correct DRAM accesses with the consequently increased simultaneous switching propagation delay the devices supports 3T timing. If this feature is invoked the device drives the received data on its outputs for thee cycles instead of one. The only exception are the QxCS[n:0]# outputs, which are the QACS0#, QACS1#, QBCS0# and QBCS1# outputs in the QuadCS disabled mode and are QCS[3:0]# in the QuadCS enabled mode.

When the device decodes the MRS command (DRAS#=0, DCAS#=0, DWE=0 and only one DCSn#=0), it will disable the Output Inversion function and pass the DRAM MRS command with an additional (one) clock delay on the appropriate QnCSx# signal to the DRAM. Back-to-back MRS command via the SSTE32882 must have a minimum of three clock delays. The SSTE32882 will automatically enable Output Inversion if there is no DRAM MRS command three clocks after the previous MRS command.

The inputs and outputs relationships for 1T timing and 3T timing are shown in Figure 14, Figure 15 and Figure 16.

2.1   Description (cont'd)

Figure 14 — 1T Timing During Normal Operation

(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Exhibit 63

JEDEC Standard No. 82-29
Page 16

2.1   Description (cont'd)

Figure 15 — 3T Timing During DRAM MRS Command

(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Exhibit 63

2.1 Description (cont'd)

Figure 16 — 3T Timing During Multiple DRAM MRS Commands

(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Exhibit 63

JEDEC Standard No. 82-29
Page 18

2.2   Control words

The SSTE32882 registers have internal control bits for adapting the configuration of certain device features. The control bits are accessed by the simultaneous assertion of both DCS0# and DCS1# in the QuadCS disabled mode. In the QuadCS enable mode, the simultaneous assertion of both DCS2# and DCS3# during normal operation, and the assertion of all four DCS[3:0]# inputs also result in control word access. However, assertion of any three DCS[3:0]# inputs is not legal. Register Qn outputs including QxCKE0, QxCKE1, QxODT0 and QxODT1 remain in their previous state. Select signals QxCS[n:0]# are set to HIGH during control word access.

The SSTE32882 allocates decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0 and DBA1. Bits DA[15:5] must be LOW and at least one DCKEn input must be HIGH for a valid access. During control word write, at least one DCKEn must be asserted. If register CKE power down feature is disabled, DCKEn input is a don't care (either HIGH or LOW). The inputs on DRAS#, DCAS#, DWE# and DODT[1:0] can be either HIGH or LOW and are ignored by the register during control word access. In all cases Address and command parity is checked during control word write operations. ERROUT# is asserted and the command is ignored if a parity error is detected. Using this mechanism, controllers may use the SSTE32882 to validate the address and command bus signal integrity to the module as long as one or more of the parity checked input signals DA3..DA15, DBA0, DBA1, DRAS#, DCAS#, DWE# are kept HIGH.

Control word access must be possible at any defined frequency independent of the current setting of RC2[DBA1] control registers.

Exhibit 63

Case 1:21-cv-01458-UNA Document 1-3 Filed 10/15/21 Page 98 of 306 PageID #: 587
Case 1:21-cv-01458-UNA Document 1-3 Filed 10/15/21 Page 98 of 306 PageID #: 587

JEDEC Standard No. 82-29

Page 19

2.3   Pinout configuration

Package options includes 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 11 x 20 grid, 8.0mm x 13.5mm. It is using the mechanical outline MO-246 variation F. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

Figure 17 — Pinout Configuration

Exhibit 63

JEDEC Standard No. 82-29
Page 20

2.3.1 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode disabled)

176-ball, 11 · 20 grid, TOP VIEW

Table 3, "Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

Table 3 — Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD		VDD	VDD	VDD		VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD		VDD	VDD	VDD		VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS#
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DODT1
T	DCKE0	DCS0#								DCS1#	DODT0
U	DA12	DBA2		Y1#	PVSS	VDD	PVDD	Y0#		DA13	DCAS#
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		DRAS#	DWE#
W	DA8	DA6	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions -- must not be connected on system
Pins Y2 and R6 are reserved for DCS2# and DCS3# in the QuadCS mode and must not be connected on system, the device design needs to tolerate this floating pin
Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

Exhibit 63

2.3.2   Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode disabled)

Table 4, "Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in back configuration with QuadCS mode disabled.

Table 4 — Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD		VDD	VDD	VDD		VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD		VDD	VDD	VDD		VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	QBRAS#
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	DCS1#								DCS0#	DCKE0
U	DCAS#	DA13		Y1#	PVSS	VDD	PVDD	Y0#		DBA2	DA12
V	DWE#	DRAS#		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	RSVD	DA7

Pins A9 and W7 are reserved for future functions -- must not be connected on system
Pin Y10 and R6 are reserved for DCS2# and DCS3# in the QuadCS mode and must not be connected on system, the device design needs to tolerate this floating pin
Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

Exhibit 63

JEDEC Standard No. 82-29
Page 22

2.3.3 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode enabled)

Table 5, "Ball Assignment; MIRROR=LOW, QCSEN#=LOW," specifies the pinout for SSTE32882 in front configuration with QuadCS mode enabled.

Table 5 — Ball Assignment; MIRROR=LOW, QCSEN#=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD		VDD	VDD	VDD		VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD		VDD	VDD	VDD		VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS#
R	DCKE1	DA14	DA15		DA5	DCS3#	DA2		DA1	DA10	DODT1
T	DCKE0	DCS0#								DCS1#	DODT0
U	DA12	DBA2		Y1#	PVSS	VDD	PVDD	Y0#		DA13	DCAS#
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		DRAS#	DWE#
W	DA8	DA6	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA0	DBA0
Y	DA7	DCS2#	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions -- must not be connected on system
Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

Exhibit 63

2.3.4 Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode enabled)

Table 6, "Ball Assignment; MIRROR=HIGH, QCSEN#=LOW," specifies the pinout for SSTE32882 in back configuration with QuadCS mode enabled.

Table 6 — Ball Assignment; MIRROR=HIGH, QCSEN#=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD		VDD	VDD	VDD		VDD	QCS3#	QABA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD		VDD	VDD	VDD		VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	QBRAS#
R	DODT1	DA10	DA1		DA2	DCS3#	DA5		DA15	DA14	DCKE1
T	DODT0	DCS1#								DCS0#	DCKE0
U	DCAS#	DA13		Y1#	PVSS	VDD	PVDD	Y0#		DBA2	DA12
V	DWE#	DRAS#		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	DCS2#	DA7

Pins A9 and W7 are reserved for future functions -- must not be connected on system
Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

Exhibit 63

2.4   Pinout configuration narrow package[1]

Optional the device is available as 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 8 x 22 grid, 6.0mm x 15mm. It is using the mechanical outline MO-246 variation B. Equivalent to the 11 x 20 grid configuration the device pinout supports outputs on the outer two left and right columns. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias.

Figure 18 — Pinout Configuration

1. This package may only be used in new DIMM designs. It is not intended for use in the existing DIMM's.

Exhibit 63

2.4.1 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode disabled)

176-ball, 8 x 22 grid, TOP VIEW

Table 7, "Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

Table 7 — Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD	VDD	VDD	VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD	VDD	VDD	VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	DCS0#	DCKE0	VSS	VSS	VSS	VSS	DODT0	DCS1#
U	DA12	DA3	Y1#	PVSS	PVDD	Y0#	DA4	DCAS#
V	DA5	DA9	Y1	PVSS	PVDD	Y0	DWE#	DA2
W	DA8	DA15	Y3#	PVSS	PVDD	Y2#	DA1	DBA0
W	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	RSVD	FBIN#	CK#	RSVD	FBOUT#	PAR_IN	DRAS#
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA0

Pins A6, AA2, AA5, AB2 and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Exhibit 63

JEDEC Standard No. 82-29
Page 26

2.4.2   Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode disabled)

Table 8, "Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in back configuration with QuadCS mode disabled.

Table 8 — Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD	VDD	VDD	VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD	VDD	VDD	VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	DCS1#	DODT0	VSS	VSS	VSS	VSS	DCKE0	DCS0#
U	DCAS#	DA4	Y1#	PVSS	PVDD	Y0#	DA3	DA12
V	DA2	DWE#	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	Y3#	PVSS	PVDD	Y2#	DA15	DA8
W	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	DRAS#	PAR_IN	FBIN#	CK#	RSVD	FBOUT#	RSVD	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA6

Pins A6, AA5, AA7, AB2 and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Exhibit 63

2.4.3 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode enabled)

Table 9, "Ball Assignment; MIRROR=LOW, QCSEN#=LOW," specifies the pinout for SSTE32882 in front configuration with QuadCS mode enabled.

Table 9 — Ball Assignment; MIRROR=LOW, QCSEN#=LOW

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD	VDD	VDD	VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD	VDD	VDD	VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	DCS0#	DCKE0	VSS	VSS	VSS	VSS	DODT0	DCS1#
U	DA12	DA3	Y1#	PVSS	PVDD	Y0#	DA4	DCAS#
V	DA5	DA9	Y1	PVSS	PVDD	Y0	DWE#	DA2
W	DA8	DA15	Y3#	PVSS	PVDD	Y2#	DA1	DBA0
W	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	DCS2#	FBIN#	CK#	RSVD	FBOUT#	PAR_IN	DRAS#
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	DCS3#	DA0

Pins A6, AA5 and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Exhibit 63

JEDEC Standard No. 82-29
Page 28

2.4.4   Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode enabled)

Table 10, "Ball Assignment; MIRROR=HIGH, QCSEN#=LOW)," specifies the pinout for SSTE32882 in back configuration with QuadCS mode enabled.
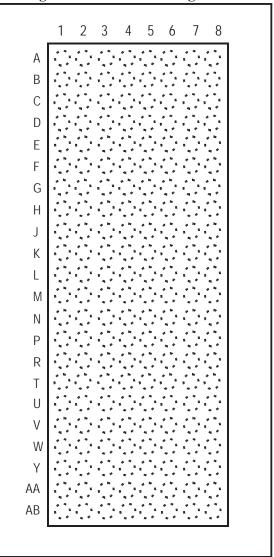
Table 10 — Ball Assignment; MIRROR=HIGH, QCSEN#=LOW)

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD	VDD	VDD	VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD	VDD	VDD	VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	DCS1#	DODT0	VSS	VSS	VSS	VSS	DCKE0	DCS0#
U	DCAS#	DA4	Y1#	PVSS	PVDD	Y0#	DA3	DA12
V	DA2	DWE#	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	Y3#	PVSS	PVDD	Y2#	DA15	DA8
W	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	DRAS#	PAR_IN	FBIN#	CK#	RSVD	FBOUT#	DCS2#	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	DCS3#	DA6

Pins A6, AA5 and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Exhibit 63

2.5   Terminal Functions

Table 11 — Terminal functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE0/1, DODT0/1	1.5/1.35V CMOS Inputs[1]	DRAM corresponding register function pins not associated with Chip Select.
Chip Select gated inputs	DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#	1.5/1.35V CMOS Inputs[1]	DRAM corresponding register inputs, re-driven only when either chip select is LOW. If both chip selects are LOW the register maintains the state of the previous input clock cycle at its outputs
Chip Select inputs	DCS0#, DCS1#	1.5/1.35V CMOS Inputs[1]	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re-driven.
	DCS2#, DCS3#	1.5/1.35V CMOS Inputs[1]	DRAM corresponding register Chip Select signals when QuadCS mode is enabled. DCS2# and DCS3# inputs are disabled when QuadCS mode is disabled.
Re-driven outputs	QxA0..QxA15, QxBA0..QxBA2, QxCS0/1#, QxCKE0/1, QxODT0/1, QxRAS#, QxCAS#, QxWE#	1.5/1.35V CMOS Outputs[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. x is A or B; outputs are grouped as A or B and may be enabled or disabled via RC0.
Parity input	PAR_IN	1.5/1.35V CMOS Input[1]	Input parity is received on pin PAR_IN and should maintain parity across the Chip Select Gated inputs (see above), at the rising edge of the input clock, one input clock cycle after corresponding data and one or both chip selects are LOW.
Parity error output	ERROUT#	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. ERROUT# will be active for two clock cycles, and delayed by 3 clock cycles to the corresponding input data
Clock inputs	CK, CK#	1.5/1.35V CMOS Inputs[1]	Differential master clock input pair to the PLL; has weak internal pull-down resistors (10K∗ ~100K∗).
Clock Outputs	Y0, Y0#.. Y3, Y3#	1.5/1.35V CMOS Outputs	Re-driven Clock
Feedback inputs	FBIN, FBIN#	1.5/1.35V CMOS Inputs[1]	Differential feedback inputs
Feedback outputs	FBOUT, FBOUT#	1.5/1.35V CMOS Outputs	Differential feedback outputs
Miscellaneous inputs	RESET#	CMOS[3]	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float. Once RESET# becomes HIGH the outputs get enabled and are driven LOW until the first access has been performed. RESET# also resets the ERROUT# signal.
	MIRROR	CMOS[3]	Selects between two different ballouts for front or back operation. When the MIRROR input is HIGH, the device input bus termination (IBT) is turned off on all inputs, except the DCSn# and DODTn inputs.
	QCSEN#	CMOS[3]	Enables the QuadCS mode. The QCSEN# input has a weak internal pullup resistor (10K∗ ~100K∗).
	VREFCA[1]	VDD/2	Input reference voltage for the data inputs.
	VDD	Power Input	Power supply voltage
	VSS	Ground Input	Ground
	AVDD	Analog Power	Analog supply voltage
	AVSS	Analog Ground	Analog ground
	PVDD	Clock Driver Output Power	Clock logic and clock output driver power supply
	PVSS	Clock Driver Output Ground	Clock logic and clock output driver ground
	RSVD	I/O	Reserved pins, must be left floating

1. 1.5/1.35V CMOS inputs uses VREFCA as the switching point reference for these receivers.
2. These outputs are optimized for memory applications to drive DRAM inputs to 1.5V or 1.35V signaling levels
3. Voltage levels according standard JESD8-11A, wide range, non terminated logic

Exhibit 63

JEDEC Standard No. 82-29
Page 30

2.6 Function Tables

Table 12 — Function table (each flip flop) with QuadCS mode disabled

	Inputs							Outputs				
RESET#	DCS0#	DCS1#	CK[1]	CK#[1]	ADDR[2]	CMD[3]	CTRL[4]	Qn	QxCS0#	QxCS1#	QxODTn	QxCKEn
H	L	L	*	*	Control Word	Control Word	Control Word	No change	H	H	No change	No change
H	X	X	L or H	H or L	X	X	X	No change	No change	No change	No change	No change
H	L	H	*	*	X	X	X	Follows Input	L	H	Follows Input	Follows Input
H	X	X	L	L	X	X	X	Float	Float	Float	Float	L
H	H	L	*	*	X	X	X	Follows Input	H	L	Follows Input	Follows Input
H	H	H	*	*	X or Float	X or Float	X	No change or Float[5]	H	H	Follows Input	Follows Input
L	X or Float	X or Float	X or Float	X or Float	X or Float	X or Float	X or Float	Float	Float	Float	Float	L

1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. ADDR = DA[15:0], DBA[2:0]
3. CMD = DRAS#, DCAS#, DWE#
4. CTRL = DODTn, DCKEn
5. Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

Table 13 — Function table (each flip flop) with QuadCS mode enabled

	Inputs				Outputs			
RESET#	DCS[3:0]#	CK[1]	CK#[1]	A/C/E[2]	Qn	QCS[3:0]#	QxODTn	QxCKEn
H	LLHH	*	*	Control Word	No change	HHHH	No change	No change
H	HHLL	*	*	Control Word	No change	HHHH	No change	No change
H	LLLL	*	*	Control Word	No change	HHHH	No change	No change
H	XXXX	L or H	H or L	X	No change	No change	No change	No change
H	LHHH	*	*	Dn	Dn	LHHH	DODTn	DCKEn
H	HLHH	*	*	Dn	Dn	HLHH	DODTn	DCKEn
H	HHLH	*	*	Dn	Dn	HHLH	DODTn	DCKEn
H	HHHL	*	*	Dn	Dn	HHHL	DODTn	DCKEn
H	LHLH	*	*	Dn	Dn	LHLH	DODTn	DCKEn
H	HLLH	*	*	Dn	Dn	HLLH	DODTn	DCKEn
H	LHHL	*	*	Dn	Dn	LHHL	DODTn	DCKEn
H	HLHL	*	*	Dn	Dn	HLHL	DODTn	DCKEn
H	XXXX	L	L	X	float	float	float	L
H	HHHH	*	*	X	No change or float[3]	HHHH	DODTn	DCKEn
H	LLLH	*	*	X	Ilegal Input States			
H	LLHL	*	*	X	Ilegal Input States			
H	LHLL	*	*	X	Ilegal Input States			
H	HLLL	*	*	X	Ilegal Input States			
L	X or float	X or float	X or float	X or float	float	float	float	L

1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. A/C/E = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, DODTn, DCKEn
3. Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

Exhibit 63

2.6   Function Tables (cont'd)

Table 14 — Parity, LOW power and Standby function table with QuadCS mode disabled

Inputs							Output
RESET#	DCS0#	DCS1#	CK^1	CK#^{1}	* of A/C^2	PAR_IN^3	ERROUT#^{4}
H	L	X	*	*	Even	L	H
H	L	X	*	*	Odd	L	L
H	L	X	*	*	Even	H	L
H	L	X	*	*	Odd	H	H
H	X	L	*	*	Even	L	H
H	X	L	*	*	Odd	L	L
H	X	L	*	*	Even	H	L
H	X	L	*	*	Odd	H	H
H	H	H	*	*	X	X	H^5
H	X	X	L or H	H or L	X	X	ERROUT#n_0
H	X	X	L	L	X	X	H^6
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

2. A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.

3. PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.

4. This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going LOW. If ERROUT# is LOW, it stays latched LOW for exactly two clock cycles or until RESET# is driven LOW.

5.Same 3 cycle delay for ERROUT# is valid for the de-select phase (see diagram)

6.The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

Exhibit 63

JEDEC Standard No. 82-29
Page 32

Table 15 — Parity, LOW power and Standby function table with QuadCS mode enabled

Inputs						Output
RESET#	DCS[3:0]#	CK[1]	CK#[1]	* of A/C[2]	PAR_IN[3]	ERROUT#[4]
H	LXXX XLXX XXLX XXXL	*	*	Even	L	H
H	LXXX XLXX XXLX XXXL	*	*	Odd	L	L
H	LXXX XLXX XXLX XXXL	*	*	Even	H	L
H	LXXX XLXX XXLX XXXL	*	*	Odd	H	H
H	HHHH	*	*	X	X	H[5]
H	XXXX	L or H	H or L	X	X	ERROUT#n_0
H	XXXX	L	L	X	X	H[6]
L	X or floating	X or floating	X or floating	X or floating	X or floating	H

1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.
3. PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.
4. This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going LOW. If ERROUT# is LOW, it stays latched LOW for exactly two clock cycles or until RESET# is driven LOW.
5. Same 3 cycle delay for ERROUT# is valid for the de-select phase (see diagram)
6. The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

Exhibit 63

2.6   Function Tables (cont'd)

Table 16 — PLL function table

Inputs					Outputs				
RESET#	AVDD	OEn^1	CK^2	$CK\#^2$	Yn	Yn#	FBOUT	FBOUT#	PLL
L	X	X	X	X	Float	Float	Float	Float	Off
H	V_{DD} nominal	L	L	H	L	H	L	H	On
H	V_{DD} nominal	L	H	L	H	L	H	L	On
H	V_{DD} nominal	H	L	H	Float	Float	L	H	On
H	V_{DD} nominal	H	H	L	Float	Float	H	L	On
H	V_{DD} nominal	X	L	L	Float	Float	Float	Float	Off
H	GND^3	L	L	H	L	H	L	H	Bypass/Off
H	GND^3	L	H	L	H	L	H	L	Bypass/Off
H	GND^3	H	L	H	Float	Float	L	H	Bypass/Off
H	GND^3	H	H	L	Float	Float	H	L	Bypass/Off
H	GND^3	X	L	L	Float	Float	Float	Float	Bypass/Off
H	X	X	H	H	Reserved				

1.The Output Enable (OEn) to disable the output buffer is not an input signal to the SSTE32882, but an internal signal from the PLL powerdown control and test logic. It is controlled by setting or clearing the corresponding bit in the Clock Driver mode register.

2.It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

3.This is a device test mode and all register timing parameter are not guaranteed.

JEDEC Standard No. 82-29
Page 34

2.7 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RC2 (bit DBA1 and DA3) and RC10, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC2: bit DBA1 and DA3, and RC10) this settling may take up to t_{STAB} time. All chip select inputs, DCS[n:0]#, must be kept HIGH during that time. The Control Words can be accessed and written to when running within any one defined frequency band.

2.7.1 Control Word Decoding

The values to be programmed into each control word are presented on signals DA3, DA4, DBA0 and DBA1 simultaneously with the assertion of the control word access through DCS0# and DCS1#, or DCS2# and DCS3# in the QuadCS enabled mode, and the address of the control word on DA0, DA1, DA2 and DBA2.

The reset default state of Control Words 0 .. 5 and Control Words 8 .. 15 is "0". The reset default state for Control Words 6 and 7 is Vendor Specific. Every time the device is reset, its default state is restored. Stopping the clocks (CK=CK#=LOW) to put the device in low-power mode will not alter the control word settings.

Table 17 — Control Word Decoding with QuadCS mode disabled

Control Word	Symbol	Signal						Meaning
		DCS0#	DCS1#	DBA2	DA2	DA1	DA0	
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Global Features Control word
Control word 1	RC1	L	L	L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2	L	L	L	L	H	L	Timing Control word
Control word 3	RC3	L	L	L	L	H	H	CA Signals Driver Characteristics Control word
Control word 4	RC4	L	L	L	H	L	L	Control Signals Driver Characteristics Control word
Control word 5	RC5	L	L	L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6	L	L	L	H	H	L	Reserved, free to use by vendor
Control word 7	RC7	L	L	L	H	H	H	Reserved, free to use by vendor
Control word 8	RC8	L	L	H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9	L	L	H	L	L	H	Power Saving Settings Control Word
Control word 10	RC10	L	L	H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11	L	L	H	L	H	H	Encoding for RDIMM Operating V_{DD}
Control word 12	RC12	L	L	H	H	L	L	Reserved for future use
Control word 13	RC13	L	L	H	H	L	H	Reserved for future use
Control word 14	RC14	L	L	H	H	H	L	Reserved for future use
Control word 15	RC15	L	L	H	H	H	H	Reserved for future use

Exhibit 63

Table 18 — Control Word Decoding with QuadCS mode enabled

Control Word	Symbol	Signal					Meaning
		DCS[3:0]#	DBA2	DA2	DA1	DA0	
None	n/a	HXHX	X	X	X	X	No control word access
None	n/a	HXXH	X	X	X	X	
None	n/a	XHHX	X	X	X	X	
None	n/a	XHXH	X	X	X	X	
None	n/a	HLLL	X	X	X	X	Ilegal Input States
None	n/a	LHLL	X	X	X	X	
None	n/a	LLHL	X	X	X	X	
None	n/a	LLLH	X	X	X	X	
Control word 0	RC0	LLHH or HHLL or LLLL	L	L	L	L	Global Features Control word
Control word 1	RC1		L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2		L	L	H	L	Timing Control word
Control word 3	RC3		L	L	H	H	CA Signals Driver Characteristics Control word
Control word 4	RC4		L	H	L	L	Control Signals Driver Characteristics Control word
Control word 5	RC5		L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6		L	H	H	L	Reserved, free to use by vendor
Control word 7	RC7		L	H	H	H	Reserved, free to use by vendor
Control word 8	RC8		H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9		H	L	L	H	Power Saving Settings Control Word
Control word 10	RC10		H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11		H	L	H	H	Encoding for RDIMM Operating V_{DD}
Control word 12	RC12		H	H	L	L	Reserved for future use
Control word 13	RC13		H	H	L	H	Reserved for future use
Control word 14	RC14		H	H	H	L	Reserved for future use
Control word 15	RC15		H	H	H	H	Reserved for future use

Exhibit 63

JEDEC Standard No. 82-29
Page 36

2.7.2 Control Word Functions

The following sections describe the contents of each control word.

Table 19 — RC0: Global Features Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Output Inversion	Output Inversion enabled
x	x	x	1		Output Inversion disabled
x	x	0	x	Floating Outputs (when DCSn# = HIGH, and DA4 = "1")	Float disabled (normal output drive strength as defined in RC3, 4, and 5)
x	x	1	x		Float enabled (or Weak Drive mode when RC9 [DA3=1])
x	0	x	x	A outputs disabled	A outputs enabled
x	1	x	x		A outputs disabled
0	x	x	x	B outputs disabled	B outputs enabled
1	x	x	x		B outputs disabled

Output floating refers to allowing many A/B outputs to enter a hi-Z state when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g., VDD, VTT, or VSS). When output floating is enabled, the following outputs (on both matching A and B outputs) are hi-Z when not actively driven: QxA0, QxA1, QxA2, QxA3, QxA4, QxA5, QxA6, QxA7, QxA8, QxA9, QxA10/AP, QxA11, QxA12/BC, QxA13, QxA14, QxA15, QxBA0, QxBA1, QxBA2, QxRAS#, QxCAS#, and QxWE#.

A or B output disable allows the use of the SSTE32882 in reduced parts count applications such as DDR3 Mini-RDIMMs. When output disable is asserted, all outputs on the corresponding side of the register including the clock drivers remain in Hi-Z at all times.

Table 20 — RC1: Clock Driver Enable Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Disable Y0/Y0# clock	Y0/Y0# clock enabled
x	x	x	1		Y0/Y0# clock disabled
x	x	0	x	Disable Y1/Y1# clock	Y1/Y1# clock enabled
x	x	1	x		Y1/Y1# clock disabled
x	0	x	x	Disable Y2/Y2# clock	Y2/Y2# clock enabled
x	1	x	x		Y2/Y2# clock disabled
0	x	x	x	Disable Y3/Y3# clock	Y3/Y3# clock enabled
1	x	x	x		Y3/Y3# clock disabled

Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on CK/CK# unless the system stops the clock inputs to the SSTE32882 to enter the lowest power mode.

Exhibit 63

.2.7.2   **Control Word Functions (cont'd)**

Table 21 — F0RC2: Timing Control Word
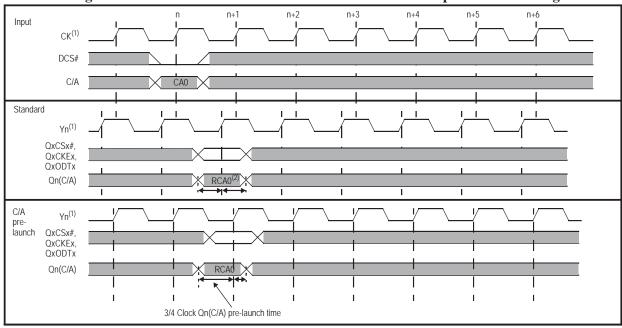
Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Address- and command-nets pre-launch (Control Signals QxCKE, QxCS, QxODT are controlled by F[1-2]RC13 & F[1-2]RC14	Standard (1/2 Clock)
x	x	x	1		Address and command nets pre-launch Controlled by F[1-2]RC12
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
x	0	x	x	Input Bus Termination	100 Ohm
x	1	x	x		150 Ohm
0	x	x	x	Frequency Band Select	Operation (Frequency Band 1)
1	x	x	x		Test Mode (Frequency Band 2)

The Input Bus Termination (IBT) is also located in this control word with two options of 100 Ohms or 150 Ohms which can be selected to adapt to different system scenarios. At power-up, the SSTE32882 IBT defaults to 100 Ohms. The system controller can reprogram the termination resistance to 150 Ohms by setting this bit. Only the DAn, DBAn, DRAS#, DCAS#, DWE#, DCSn#, DODT, DCKEn and PAR_IN inputs have the IBT. The CK, CK#, FBIN, FBIN#, RESET# and MIRROR inputs do not have IBT.

If MIRROR is 'HIGH' then it is assumed the register is located on the back side of a module where two registers are tied together on the input side. In this case, for the register on the back side, IBT are turned off on all inputs, except the DCSn# and DODTn inputs.

The following diagram illustrates the pre-launch feature whereby double loaded nets in a 2-rank configuration can be driven with an earlier signal compared to output clock and control in order to compensate for the slower signal travel speed. This timing applies at all supported frequencies.

JEDEC Standard No. 82-29

Page 38

2.7.2 Control Word Functions (cont'd)

Figure 19 — Standard versus Address and Command-Nets pre-launch Timing

(1) CK# and Yn# left out for better visibility

(2) RCA0 is re-driven command address signal based on input CA0

1. DCS[n:0]# indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled.
   QxCS[n:0] indicates all of the chip select outputs.

Exhibit 63

2.7.2   Control Word Functions (cont'd)

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals =QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#
- Control Signals = QxCSn#, QxCKEn, QxODTn
- CK = Yn .. Yn#

2.8   Register Output Slew-Rate & R-on Targets for Each Drive Strength

Table 22 — Output Slew-Rate & R-on Targets

Drive Settings	Output Driver R-on Targets (Ohms)			Output Slew-Rate (V/ns)					
				Range (1.5V) DDR3-800/1066/1333		Range (1.5V) DDR3-1600		Range (1.35V) DDR3L-800/1066/1333/1600	
	Min	Nom	Max	Min	Max	Min	Max	Min	Max
Light	22	26	30	2	7	2	5	1.8	4.5
Moderate	16	19	22	2	7	2	5	1.8	4.5
Strong	12	14	16	2	7	2	5	1.8	4.5

Table 23 — RC3: CA Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Command/Address Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	Command/Address Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Reserved

1. DCS[n:0]# indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled.
QxCS[n:0] indicates all of the chip select outputs.

Exhibit 63

JEDEC Standard No. 82-29
Page 40

2.7.2   Control Word Functions (cont'd)

Table 24 — RC4: Control Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Control Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Reserved
x	x	1	1		Reserved
0	0	x	x	Control Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Reserved
1	1	x	x		Reserved

Table 25 — RC5: CK Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Clock Y1, Y1#, Y3, and Y3# Output Drivers	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	Clock Y0, Y0#, Y2, and Y2# Output Drivers	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Reserved

Exhibit 63

2.7.2   Control Word Functions (cont'd)

Table 26 — RC8 - Additional IBT Setting Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	IBT Compatibility Settings	IBT as defined in RC2
0	x	x	x	Mirror Mode	IBT Off when MIRROR is 'HIGH'[1]
1	x	x	x		IBT On when MIRROR is 'HIGH'[2]
x	0	0	1	Input Bus Termination[1]	Reserved
x	0	1	0		200 Ohm
x	0	1	1		Reserved
x	1	0	0		300 Ohm
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Off[3]

1. If MIRROR is 'HIGH' then Input Bus Termination (IBT) is turned off on all inputs, except DCSn# and DODTn inputs.
2. When DBA0 = 1, DA4 = 1, DA3 = 1, IBT on all inputs is turned off irrespective of DBA1 setting.
3. With this setting, irrespective of the logic level of the MIRROR input pin, IBT on all inputs (including DCSn# and DODTn) is turned off.

Table 27 — RC9: Power Saving Settings Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Weak Drive Mode[1]	"Floating Outputs" as defined in RC0 [DA4]
x	x	x	1	(when DCSn# = HIGH, DA3=1, and RC0 [DA4=1])	Weak Drive enabled Weak Drive Impedance: 70 Ohm (min), 100 Ohm (nom), 120 Ohm (max)
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
1	0	x	x	CKE Power Down Mode	CKE power down with IBT ON, QxODT is a function of DxODT
1	1	x	x		CKE power down with IBT off, QxODT held LOW
0	x	x	x	CKE Power Down Mode Enable	Disabled
1	x	x	x		Enabled

1. When all DCS# pins are HIGH (i.e. SDRAM is in deselected state), there is no memory access to the DRAM, and the Register output can either be in a Normal Drive Mode, floated, or driven under Weak Drive Mode. A Weak Drive Mode is a mode in which CA signal output drivers (QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#) will be driven 2.5 to 3 times weaker than the Light Drive as specified in RC3, and the SDRAM VIL/VIH DC limit will be maintained. The Weak Drive Mode entry and exit timing is bounded by tDIS and tEN respectively.

The SSTE32882 register supports different power down modes. By default, the Power Down feature is disabled (RC9[DBA1]=0). The register ignores CKE Power Down mode setting when this function is disabled. If the CKE Power Down mode is enabled (RC9[DBA1]=1), then power down is invoked once both DCKE0 and DCKE1 are LOW. Bit DBA0 selects how IBT and ODT behaves.

Exhibit 63

JEDEC Standard No. 82-29
Page 42

2.7.2   Control Word Functions (cont'd)

Table 28 — RC10: Encoding for RDIMM Operating Speed

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	f ≤ 800 MTS	DDR3/DDR3L-800 (default)
x	0	0	1	800 MTS < f ≤ 1066 MTS	DDR3/DDR3L-1066
x	0	1	0	1066 MTS < f ≤ 1333 MTS	DDR3/DDR3L-1333
x	0	1	1	1333 MTS < f ≤ 1600 MTS	DDR3/DDR3L-1600
x	1	0	0	Reserved	Reserved
x	1	0	1	Reserved	Reserved
x	1	1	0	Reserved	Reserved
x	1	1	1	Reserved	Reserved

NOTE   The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run.

RC11 will be used to inform SSTE32882 under what operating voltage V_{DD} will be used. Register can use the information to optimize their functionality and performance at DDR3L conditions.
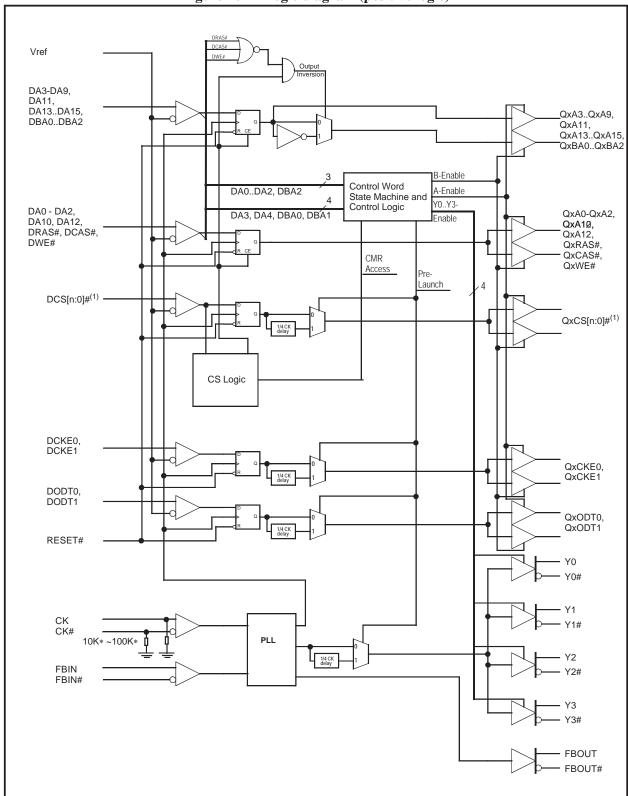
Table 29 — RC11: Operating Voltage VDD Control Word[1]

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Register V_{DD} Operating Voltage	DDR3 1.5V mode
x	x	0	1		DDR3L 1.35V mode
x	x	1	0		Reserved
x	x	1	1		Reserved
0	0	x	x		Reserved
0	1	x	x		Reserved
1	0	x	x		Reserved
1	1	x	x		Reserved

1. DDR3L 1.35V register is backward compatible and operable to DDR3 1.5V specification. To guarantee all timings and specifications for DDR3 1.5V, the register must be configured with RC11[DA4:DA3]=00b.

Exhibit 63

2.9   Logic diagram

Figure 20 — Logic diagram (positive logic)

Exhibit 63

JEDEC Standard No. 82-29
Page 44
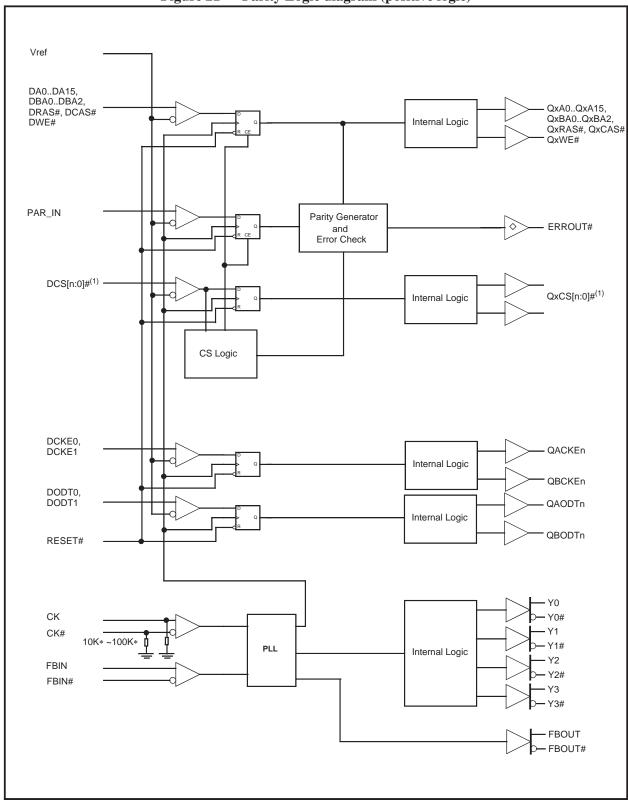
2.9   Logic Diagram (cont'd)

Figure 21 — Parity Logic diagram (positive logic)

Exhibit 63

2.10   Absolute maximum ratings

Table 30 — Absolute maximum ratings over operating free-air temperature range [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		−0.4	+1.975	V
V_I	Receiver input voltage	See Note 2 and 3	−0.4	V_{DD} + 0.5	V
V_{REF}	Reference voltage		−0.4	V_{DD} + 0.5	V
V_O	Driver output voltage	See Note 2 and 3	−0.4	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	-	-50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	-	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	Storage temperature		−65	+150	×C

NOTE 1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 1.975 V maximum.

Exhibit 63

JEDEC Standard No. 82-29
Page 46

2.11   DC and AC Specifications

The SSTE32882 parametric values are specified for the device default control word settings, unless otherwise stated.
Note that the RC10 setting does not affect any of the parametric values.

Table 31 — Operating Electrical Characteristics

Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage (1.5V Operation)		1.425	1.5	1.575	V
	DC Supply voltage (1.35V Operation)		1.282	1.35	1.451	V
V_{REF}	DC Reference voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
V_{TT}	DC Termination voltage		V_{REF} − 40 mV	V_{REF}	V_{REF} + 40 mV	V
$V_{IH(AC)}$	AC HIGH-level input voltage (1.5V Operation, DDR3-800/1066/1333)	Data inputs[1]	V_{REF} + 175 mV	–	V_{DD} + 0.4	V
	AC HIGH-level input voltage (1.5V Operation, DDR3-1600)	Data inputs[1]	V_{REF} + 150 mV	–	V_{DD} + 0.4	V
	AC HIGH-level input voltage (1.35V Operation, DDR3L-800/1066/1333)	Data inputs[1]	V_{REF} + 150 mV	–	V_{DD} + 0.2	V
	AC HIGH-level input voltage (1.35V Operation, DDR3L-1600)	Data inputs[1]	V_{REF} + 135 mV	–	V_{DD} + 0.2	V
$V_{IL(AC)}$	AC LOW-level input voltage (1.5V Operation, DDR3-800/1066/1333)	Data inputs[1]	−0.4	–	V_{REF} − 175 mV	V
	AC LOW-level input voltage (1.5V Operation, DDR3-1600)	Data inputs[1]	−0.4	–	V_{REF} − 150 mV	V
	AC LOW-level input voltage (1.35V Operation, DDR3L-800/1066/1333)	Data inputs[1]	−0.2	–	V_{REF} − 150 mV	V
	AC LOW-level input voltage (1.35V Operation, DDR3L-1600)	Data inputs[1]	−0.2	–	V_{REF} − 135 mV	V
$V_{IH(DC)}$	DC HIGH-level input voltage (1.5V Operation)	Data inputs[1]	V_{REF} + 100 mV	–	V_{DD} + 0.4	V
	DC HIGH-level input voltage (1.35V Operation)	Data inputs[1]	V_{REF} + 90 mV	–	V_{DD} + 0.2	V
$V_{IL(DC)}$	DC LOW-level input voltage (1.5V Operation)	Data inputs[1]	−0.4	–	V_{REF} − 100 mV	V
	DC LOW-level input voltage (1.35V Operation)	Data inputs[1]	−0.2	–	V_{REF} − 90 mV	V
$V_{IH(CMOS)}$	HIGH-level input voltage	CMOS inputs[2]	0.65 x VDD	–	V_{DD}	V
$V_{IL(CMOS)}$	LOW-level input voltage	CMOS inputs[2]	0	–	0.35 x VDD	V
$V_{IL\,(Static)}$	Static LOW-level input voltage[3]	CK, CK#,	-	–	0.35 x VDD	V
$V_{IX(AC)}$	Differential input crosspoint voltage range (1.5V Operation, DDR3-800/1066/1333/1600)	CK, CK#, FBIN, FBIN#	0.5xV_{DD} - 175 mV	0.5 x V_{DD}	0.5xV_{DD} + 175 mV	V
			0.5xV_{DD} - 200 mV[4]	0.5 x V_{DD}	0.5xV_{DD} + 200 mV[4]	V
	Differential input crosspoint voltage range (1.35V Operation, DDR3L-800/1066/1333/1600)	CK, CK#, FBIN, FBIN#	0.5xV_{DD} - 150 mV	0.5 x V_{DD}	0.5xV_{DD} + 150 mV	V
			0.5xV_{DD} - 180 mV[5]	0.5 x V_{DD}	0.5xV_{DD} + 180 mV[5]	V
$V_{ID(AC)}$	Differential input voltage[6] (1.5V Operation, DDR3-800/1066/1333)	CK, CK#	350	–	V_{DD}	mV
	Differential input voltage[6] (1.5V Operation, DDR3-1600)	CK, CK#	300	–	V_{DD}	mV
	Differential input voltage[6] (1.35V Operation, DDR3-800/1066/1333)	CK, CK#	300	–	V_{DD}	mV
	Differential input voltage[6] (1.35V Operation, DDR3-1600)	CK, CK#	270	–	V_{DD}	mV
I_{OH}	HIGH-level output current[7]	All outputs except ERROUT#	-11	–	–	mA
I_{OL}	LOW-level output current[7]	All outputs except ERROUT#	11	–	---	mA
I_{OL}	LOW-level output current	ERROUT#	25	–	–	mA
V_{OD}	Differential re-driven clock swing (1.5V Operation)	Yn, Yn#	500	–	V_{DD}	mV
	Differential re-driven clock swing (1.35V Operation)	Yn, Yn#	450	–	V_{DD}	mV
V_{OX}	Differential Output Crosspoint Voltage (1.5V Operation)	Yn, Yn#	0.5xV_{DD} − 100 mV	–	0.5xV_{DD} + 100 mV	V
	Differential Output Crosspoint Voltage (1.35V Operation)	Yn, Yn#	0.5xV_{DD} − 90 mV	–	0.5xV_{DD} + 90 mV	V
		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	
$T_{case\,(max)}$	Case temperature[8]	109[9]	108[9]	106[9]	103[9]	ºC

1. DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW.
2. RESET#, MIRROR
3. This spec applies only when both CK and CK# are actively driven LOW. It does not apply when CK/CK# are floating.
4. Extended range for Vix is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-275 mV, and when the differential slew rate of CK - CK# is larger than 4 V/ns.
5. Extended range for Vix is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - CK# is larger than 3.6 V/ns.
6. **VID is the magnitude of the difference between the input level on CK and the input level on CK# See Diagram (Figure 29, "Voltage waveforms; input clock")**
7. Default settings
8. Measurement procedure JESD51-2
9. This spec is meant to guarantee a Tj of 125C by the SSTE32882 device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a SSTE32882 device shall not be higher than 125 ºC.

Exhibit 63

2.12 DC Specifications, IDD Specifications

Table 32 — DC Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	I_{OH} = −11 mA	V_{DD}-0.4	-	-	V
V_{OL}	Output LOW voltage	I_{OL} = 11 mA	-	-	0.4	V
V_{OL}	Output LOW voltage ERROUT#	I_{OL} = 25 mA	-	-	0.4	V
I_I	Input current	RESET#, MIRROR, $V_I = V_{DD}$ or GND	-	-	±5	∗A
I_I	Input current	QCSEN#, $V_I = V_{DD}$ or GND	-150		5	∗A
I_{ID}	Input current	Data inputs[1], $V_I = V_{DD}$ or GND	-	-	±TBD	∗A
I_{ID}	Input current	CK, CK#[2]; $V_I = V_{DD}$ or GND	-5		150	∗A
I_{DD}	Static standby current	RESET# = GND and CK, CK# = V_{IL}	-	-	5	mA
	Static operating current	RESET# = V_{DD}, MIRROR=V_{DD}, IBT OFF, Clock inputs not switching (held static LOW), $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	TBD	mA
I_{DDD}	Dynamic operating current — input clock only	RESET# = V_{DD}; MIRROR=V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and CK# switching at 50% duty cycle. I_O = 0; $V_{DD} = V_{DD}$(max)	-	vs[3]	-	mA/MHz
	Dynamic operating current — per each data input	RESET# = V_{DD}; MIRROR=VDD, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and CK# switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. I_O = 0; $V_{DD} = V_{DD}$(max)	-	vs[3]	-	mA/MHz

1. DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are measured while RESET# pulled LOW.
2. The CK and CK# inputs have internal pull-down resistors in the range of 10K∗ to 100K∗.
3. Vendor Specific, must be supplied by register vendor for full device description.

Table 33 — Capacitance values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input capacitance, Data inputs	see footnote[1,2]	1.5	-	2.5	pF
	Input capacitance, CK, CK#, FBIN, FBIN#	see footnote[1]	1.5	-	2.5	pF
C_O	Output capacitance, Re-driven and Clock Outputs	QxA0..QxA15, QxBA0..QxBA2, QxCS0/1#, QxCKE0/1, QxODT0/1, QxRAS#, QxCAS#, QxWE#, Y0, Y0#.. Y3, Y3#	1	-	2	pF
$C_{I∗}$	Delta capacitance over all inputs		-	-	0.5	pF
C_{IR}	Input capacitance, RESET#, MIRROR, QCSEN#	$V_I = V_{DD}$ or GND; V_{DD} = 1.5V	-	-	3	pF

1. This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with VDD, VSS, AVDD, AVSS, PVDD, PVSS, V_{REF} applied and all other pins (except the pin under test) floating. Input capacitance are measured with the device default settings when MIRROR=LOW.
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW.
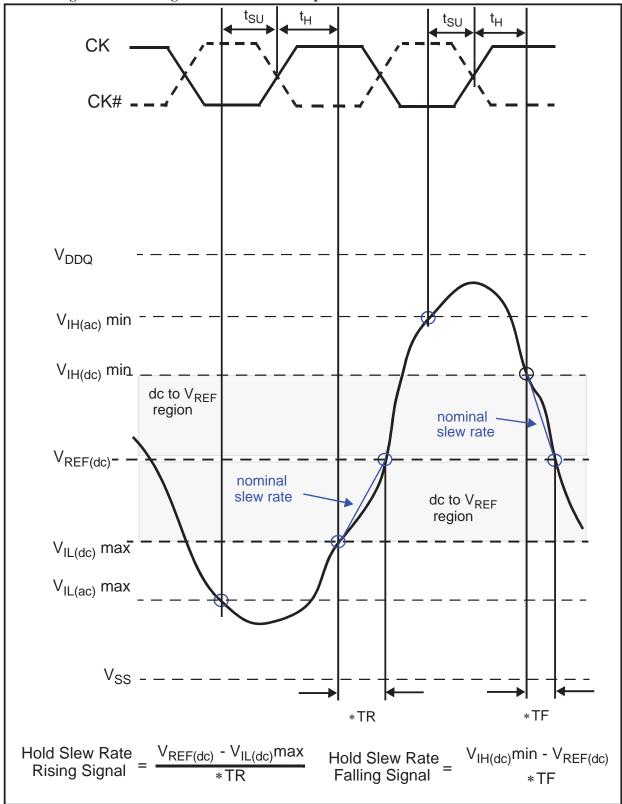
Exhibit 63

JEDEC Standard No. 82-29
Page 48

2.13   Timing Requirements

<p align="center">Table 34 — Timing requirements</p>

Symbol	Parameter	Conditions	DDR3/DDR3L-800/1066/1333		DDR3/DDR3L-1600		Unit
			Min	Max	Min	Max	
f_{clock}	Input clock frequency	application frequency[1]	300	670	300	810	MHz
f_{TEST}	Input clock frequency	Test frequency[2]	70	300	70	300	MHz
t_{CH}/t_{CL}	Pulse duration, CK, CK# HIGH or LOW		0.4	-	0.4	-	t_{CK}[3]
t_{ACT}	Inputs active time[4] before RESET# is taken HIGH	DCKE0/1=LOW and DCS[n:0]#=HIGH	8	-	8	-	t_{CK}[3]
t_{MRD}	Command word to command word programming delay	Number of clock cycles between two command programming accesses	8	-	8	-	t_{CK}[3]
t_{InDIS}	Input buffers (except for CK/CK#, DCKEn, DODTn and RESET#) disable time after DCKE[1:0] is LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling; RC9[DBA1]=1 and RC9[DBA0]= 0 or 1	1	4	1	4	t_{CK}[3]
t_{QDIS}	Output buffers (except for Yn/Yn#, QxCKEn, QxODTn and FBOUT/FBOUT#) hi-z after QxCKEn is driven LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = toggling; RC9[DBA1]=1 and RC9[DBA0]=0 or 1	1.5	1.5	1.5	1.5	t_{CK}[3]
t_{CKoff}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/CK# are driven LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling	5	-	5	-	t_{CK}
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after Ck/CK# = LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = LOW	2	-	2	-	t_{CK}
$t_{Fixedoutput}$	Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state)	RC9[DBA1]=1 and RC9[DBA0]=0 or 1	1	3	1	4	t_{CK}[3]
t_{SU}	Setup time[5]	Input valid before CK/CK#	100	-	50	-	ps
t_H	Hold time[6]	Input to remain valid after CK/CK#	175	-	125	-	ps

1.   All specified timing parameters apply
2.   Timing parameters specified for frequency band 2 apply
3.   Clock cycle time
4.   This parameter is not necessarily production tested (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation").
5.   Setup (t_{SU}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and first crossing of $V_{IH(ac)}$min. Setup (t_{SU}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation"). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation").
6.   Hold (t_H) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_H) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$ (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation"). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation").

<p align="center">Exhibit 63</p>

2.13   Timing Requirements (cont'd)

Figure 22 — Voltage Waveforms for Setup and Hold Times–Hold Time Calculation

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}\text{max}}{*TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}\text{min} - V_{REF(dc)}}{*TF}$$

Exhibit 63

JEDEC Standard No. 82-29
Page 50

2.13   Timing Requirements (cont'd)

Figure 23 — Voltage Waveforms for Setup and Hold Times–Setup Time Calculation
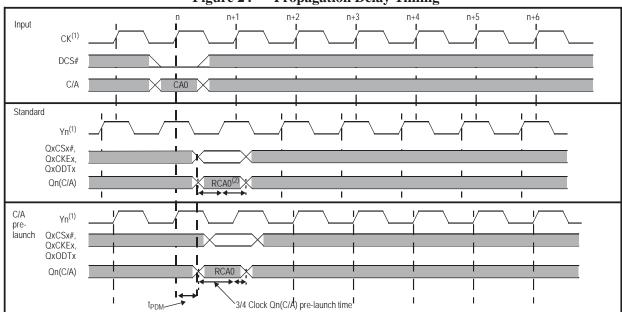
$$\text{Setup Slew Rate} \atop \text{Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{*TF}$$

$$\text{Setup Slew Rate} \atop \text{Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{*TR}$$

Exhibit 63

2.14 AC Specifications

Table 35 — Output timing requirements (see section 3.1)[1]

Symbol	Parameter	Conditions	DDR3/DDR3L-800/ 1066/1333		DDR3/DDR3L-1600		Unit
			Min	Max	Min	Max	
t_{PDM}	Propagation delay, single-bit switching (1.5V Operation)	CK/CK# to output[2]	0.65	1.0	0.65	1.0	ns
	Propagation delay, single-bit switching (1.35V Operation)[3]		0.65	1.2	0.65	1.2	ns
t_{DIS}	Output disable time (1/2-Clock pre-launch)	Yn/Yn# to output float[4]	0.5 + tQSK1(min)	-	0.5 + tQSK1(min)	-	ps
	Output disable time (3/4-Clock pre-launch)		0.25 + tQSK2(min)	-	0.25 + tQSK2(min)	-	ps
t_{EN}	Output enable time (1/2-Clock pre-launch)	Output driving to Yn/Yn#	0.5 - tQSK1(max)	-	0.5 - tQSK1(max)	-	ps
	Output enable time (3/4-Clock pre-launch)		0.75 - tQSK2(max)	-	0.75 - tQSK2(max)	-	ps

1. See diagram (Figure 30, "Qn and Yn Load circuit for propagation delay and slew measurement")
2. See diagram (Figure 24, "Propagation Delay Timing")
3. t_{PDM} range (t_{PDM_max} - t_{PDM_min}) must remain as 350ps. For example, if t_{PDM_min} for a device is 0.65ns, it's t_{PDM_max} cannot be more than 1.0ns. If t_{PDM_max} for a device is 1.2ns, it's t_{PDM_min} cannot be less than 0.85ns.
4. See diagram (Figure 32, "Voltage waveforms address floating")

Figure 24 — Propagation Delay Timing

(1) CK# and Yn# left out for better visibility
(2) RCA0 is re-driven command address signal based on input CA0

Exhibit 63

JEDEC Standard No. 82-29
Page 52

2.15   Output Buffer Characteristics

Table 36 — Output edge rates over specified operating free-air temperature range

Symbol	Parameter	Conditions	DDR3/DDR3L-800/1066/1333		DDR3/DDR3L-1600		Unit
			Min	Max	Min	Max	
dV/dt_r	rising edge slew rate [1](1.5V Operation)		2	7	2.0	5.0	V/ns
	rising edge slew rate [1](1.35V Operation)		1.8	4.5	1.8	4.5	V/ns
dV/dt_f	falling edge slew rate [1](1.5V Operation)		2	7	2.0	5.0	V/ns
	falling edge slew rate [1](1.35V Operation)		1.8	4.5	1.8	4.5	V/ns
dV/dt_D[2]	absolute difference between dV/dt_r and dV/dt_f [1]		-	1	-	1	V/ns

1. Measured into test load at default register setting
2. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

2.16   Input Buffer Characteristics

Table 37 — Input IBT characteristics over specified operating free-air temperature range

Symbol	Parameter	Conditions	DDR3/DDR3L-800/1066/1333/1600		Unit
			Min	Max	
$R_{IBT(tol)}$	Total Effective IBT Value Tolerance [1]		-10	10	%
R_{IBT*}	Total Effective IBT Value Tolerance [2]		-	5	%

1. Example for 100 ohm, Min = 90 ohm, Max = 110 ohm
2. $(1 - R_{IBT-UP}/R_{IBT-DOWN}) * 100\% <= ABS(5\%)$

Exhibit 63

2.17 Clock Driver Characteristics

Table 38 — Clock driver Characteristics at application frequency (frequency band 1)

Symbol	Parameter	Conditions	DDR3/ DDR3L-800		DDR3/ DDR3L-1066		DDR3/ DDR3L-1333		DDR3/ DDR3L-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{jit}(cc+)$	Cycle-to-cycle period jitter		0	40	0	40	0	40	0	30	ps
$t_{jit}(cc-)$	Cycle-to-cycle period jitter		-40	0	-40	0	-40	0	-30	0	ps
t_{STAB}	Stabilization time		-	6	-	6	-	6	-	6	us
t_{fdyn}	Dynamic phase offset		-50	50	-50	50	-50	50	-40	40	ps
t_{CKsk}	Fractional Clock Output skew[1]		-	15	-	15	-	15	-	10	ps
$t_{jit}(per)$	Yn Clock Period jitter		-40	40	-40	40	-40	40	-30	30	ps
$t_{jit}(hper)$	Half period jitter		-50	50	-50	50	-50	50	-40	40	ps
$t_{PWH/PWL}$	Yn pulse width HIGH/LOW duration[2]	$t_{PW} = 1/2tCK - |t_{jit}(hper)min|$ to $1/2tCK + |t_{jit}(hper)max|$	1.200	1.300	0.888	0.988	0.700	0.800	0.585	0.665	ns
t_{Qsk1}[3]	Qn Output to Yn clock tolerance (Standard 1/2-Clock Pre-Launch)	Output Inversion enabled	-100	200	-100	200	-100	200	-100	100	ps
		Output Inversion disabled	-100	300	-100	300	-100	300	-100	200	
t_{Qsk2}[4]	Qn Output to Yn clock tolerance (3/4 Clock Pre-Launch)	Output Inversion enabled	-100	200	-100	200	-100	200	-100	100	ps
		Output Inversion disabled	-100	300	-100	300	-100	300	-100	200	
t_{staoff}	Average delay through the register between the input clock and output clock[5]. (1.5V Operation)	Standard 1/2-Clock Pre-Launch $t_{staoff} = t_{PDM} + 1/2\ tCK$	1.90	2.25	1.59	1.94	1.40	1.75	1.28	1.63	ns
		3/4 Clock Pre-Launch $t_{staoff} = t_{PDM} + 3/4\ tCK$	2.53	2.88	2.06	2.41	1.77	2.12	1.59	1.94	ns
	Average delay through the register between the input clock and output clock[5]. (1.35V Operation)	Standard 1/2-Clock Pre-Launch $t_{staoff} = t_{PDM} + 1/2\ tCK$	1.90	2.45	1.59	2.14	1.40	1.95	1.28	1.83	ns
		3/4 Clock Pre-Launch $t_{staoff} = t_{PDM} + 3/4\ tCK$	2.53	3.08	2.06	2.61	1.77	2.32	1.59	2.14	ns
t_{dynoff}[6]	Maximum variation in delay between the input & output clock		-	160	-	130	-	110	-	90	ps

1. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 26, "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between Y0/Y0# and Y2/Y2#, as well as left side of the clock pairs between Y1/Y1# and Y3/Y3#. This is not a tested parameter and has to be considered as a design goal only.

2. This parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on t_{PW}.

3. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 27, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.

4. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 28, "Qn Output Skew for 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.

5. This parameter measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. t_{staoff} may vary by the amount of t_{dynoff} based on voltage and temperature drift as well as tracking error and jitter. Including this variation t_{staoff} may not exceed the limits set by $t_{staoff(min)}$ and $t_{staoff(max)}$

6. See Figure 25, "Definition for t_{staoff} and t_{dynoff}"

Exhibit 63

JEDEC Standard No. 82-29
Page 54

2.17 Clock Driver Characteristics (cont'd)

Table 39 — Clock driver Characteristics at application frequency (frequency band 1)

Symbol	Parameter	Conditions	DDR3/DDR3L-800		DDR3/DDR3L-1066		DDR3/DDR3L-1333		DDR3/DDR3L-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
The PLL in the SSTE32882 must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:											
	SSC modulation frequency		30	33	30	33	30	33	30	33	kHz
	SSC clock input frequency deviation		0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	%
SSTE32882 PLL designs should target the values below to improve tracking between CK/CK# and Yn/Yn#:											
t_{band}	PLL Loop bandwidth (-3 dB from unity gain)		25^1	-	30^1	-	35^1	-	40^1	-	Mhz

1. Implies a -3 dB bandwidth and jitter peaking of 3 dB.

Figure 25 — Definition for t_{staoff} and t_{dynoff}

1. t_{staoff} = propagation delay for clock signal (rising CK input clock edge to rising Yn output clock edge).

2. t_{dynoff} = maximum t_{staoff} variation over voltage and temperature.
   This includes all sources of jitter and drift (e.g.Thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

2.17 Clock Driver Characteristics (cont'd)

Figure 26 — Clock Output (Yn) Skew
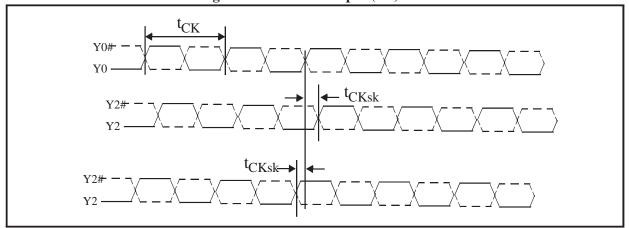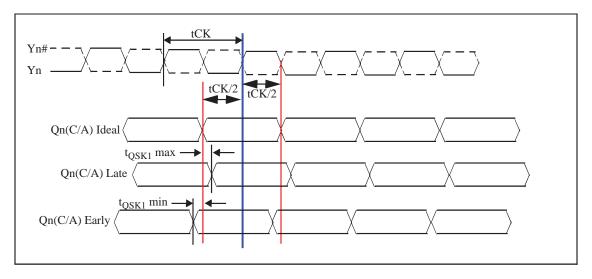
Figure 27 — Qn Output Skew for Standard 1/2-Clock Pre-Launch

Exhibit 63

JEDEC Standard No. 82-29
Page 56

2.17   Clock Driver Characteristics (cont'd)

Figure 28 — Qn Output Skew for 3/4-Clock Pre-Launch

Table 40 — Clock driver Characteristics at test frequency (frequency band 2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{jit}(cc)$	Cycle-to-cycle period jitter		0	160	ps
t_{STAB}	Stabilization time		-	15	us
t_{CKsk}	Total Clock Output Skew[1]			100	ps
	Fractional Clock Output skew[2]			vs[3]	ps
$t_{jit}(per)$	Yn Clock Period jitter		-160	160	ps
$t_{jit}(hper)$	Half period jitter		-200	200	ps
t_{Qsk1}[4]	Qn Output to clock tolerance (Standard 1/ 2-Clock Pre-Launch)	Output Inversion enabled	-100	vs[3]	ps
		Output Inversion disabled	-100	vs[3]	
t_{Qsk2}[5]	Output clock tolerance (3/4 Clock Pre-Launch)	Output Inversion enabled	-100	vs[3]	ps
		Output Inversion disabled	-100	vs[3]	
t_{dynoff}	Maximum re-driven dynamic clock offset[6]		-500	500	ps

1. This skew represents the absolute output clock skew and contains the pad skew and package skew.
2. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 26, "Clock Output (Yn) Skew")
3. Vendor Specific
4. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 27, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.
5. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 28, "Qn Output Skew for 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.
6. The re-driven clock signal is ideally centered in the address/control signal eye. This parameter describes the dynamic deviation from this ideal position including jitter and dynamic phase offset.

Exhibit 63

3 Test circuits and switching waveforms

3.1 Parameter measurement information

All input pulses are supplied by generators having the following characteristics: 300MHz ∗ PRR ∗ 810MHz; Z_O = 50 ∗ ; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

Figure 29 — Voltage waveforms; input clock

Figure 30 — Qn and Yn Load circuit for propagation delay and slew measurement

(1) C_L is parasitic (probe and jig capacitance)

Figure 31 — Voltage waveforms; propagation delay times

$V_{TT} = V_{DD}/2$

V_{ICR} Cross Point Voltage

$V_{i(P-P)}$ = 500mV (1.5V Operation) or 450mV (1.35V Operation).

t_{PDM1}, t_{PDM2} the larger number of both has to be taken when performing t_{PDM} max measurement, the smaller number of both has to be taken when performing t_{PDM} min measurement

Exhibit 63

JEDEC Standard No. 82-29
Page 58

3.1   Parameter measurement information (cont'd)

Figure 32 — Voltage waveforms address floating

1. See Figure 33, "Calculating the virtual VTT crossing point"

Enabling and disabling the CA outputs must not violate DRAM setup and hold time requirements. Therefore a t_{DIS} transition may not occur earlier than the earliest (HL/LH) transition and a t_{EN} transition may not occur later than the latest (HL/LH) transition. Regular transitions are measured between CK/CK# and CA/V_{TT} crossings however a V_{TT} crossing is not available in the state where the outputs are Hi-Z. To allow a correct and not overly conservative measurement a virtual V_{TT} crossing point is defined below. The calculation of the virtual V_{TT} crossing point is shown in Figure 31. The voltage levels for y_{xa} and y_{xb} are measured from V_{TT} ($V_{DD}/2$) and should be selected such that the region between t1 and t2 covers a linear range and represents a typical slope of the waveform within the transition area. They have to be used signed in the formula.

Exhibit 63

3.1 Parameter measurement information (cont'd)

Figure 33 — Calculating the virtual VTT crossing point
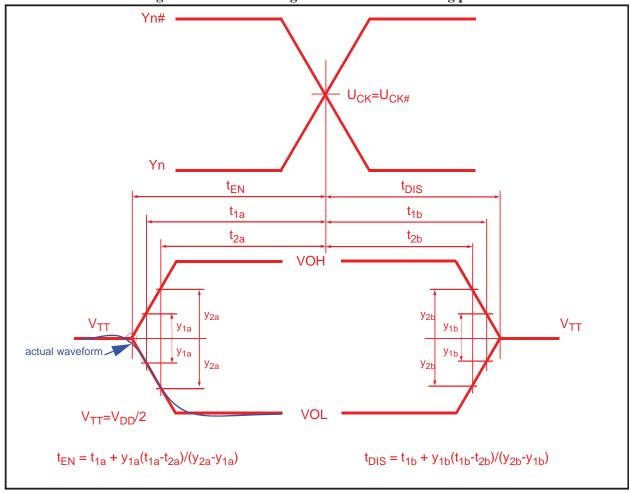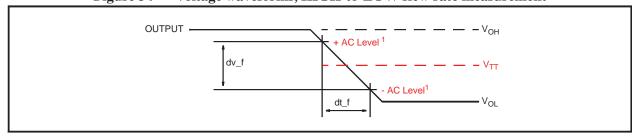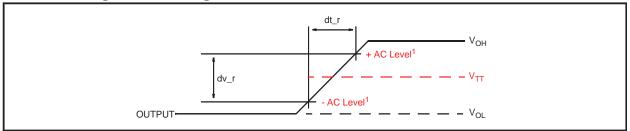
$$t_{EN} = t_{1a} + y_{1a}(t_{1a}-t_{2a})/(y_{2a}-y_{1a})$$

$$t_{DIS} = t_{1b} + y_{1b}(t_{1b}-t_{2b})/(y_{2b}-y_{1b})$$

Figure 34 — Voltage waveforms, HIGH-to-LOW slew rate measurement

1. See Table 41.

JEDEC Standard No. 82-29
Page 60

3.1 Parameter measurement information (cont'd)

Figure 35 — Voltage waveforms, LOW-to-HIGH slew rate measurement

1. See Table 41
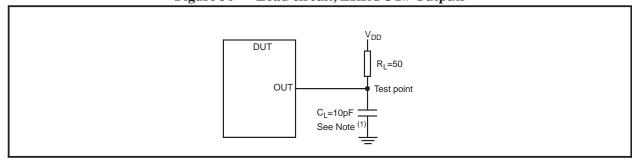
Table 41 — AC level for Slew Rate Measurement

	DDR3/DDR3L-800/1066/1333/1600
AC Level (1.5V)	150 mV
AC Level (1.35V)	135 mV

3.2 Error output load circuit and voltage measurement information

All input pulses are supplied by generators having the following characteristics: 300MHz $*$ PRR $*$ 810MHz; $Z_O = 50 *$; input slew rate = 1 V/ns $\pm$ 20%, unless otherwise specified.

Figure 36 — Load circuit, ERROUT# Outputs

(1) C_L includes probe and jig capacitance.

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

CA Signals = QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#

Control Signals = QxCSn#, QxCKEn, QxODTn

CK = Yn .. Yn#

Exhibit 63

---

4   Recommended Filtering for the Analog Power supply (AVDD)

Figure 37 — AVDD Filtering

Place the 2200pF capacitor close to the PLL

Use a wide trace for the PLL analog power & ground. Connect PLL & caps to AGND trace & connect trace to one GND via (farthest from PLL).

Bead: 0.8 Ohm DC max, 600 Ohms @ 100 MHz

Exhibit 63

JEDEC Standard No. 82-29
Page 62

---

5   Feedbackloop Topology for Registers with External Feedback

---

The SSTE32882 registering clock driver feedback path provides, when used by the device, compensation for drift caused by voltage and temperature effects. The flight time of the unloaded trace from FBOUT to FBIN must be 95 ± 15 ps to assure proper operation.

Figure 38, "External feedback loop" shows a topology proposal with the corresponding mechanical and electrical dimensions as per Table 42, "Feedback loop mechanical dimensions,". Both figure and table are for reference only. Actual values may vary according to application requirements. The overall loop length in this example is in the range of 15 mm which fits a typical DIMM stack-up The feedback loop doesn't affect post-register timing. It influences the phase relationship between pre- and post-register signalling. The register manufacturer guarantees the specified propagation delay if the user follows the feedback loop topology proposal in this paragraph.

.

Figure 38 — External feedback loop

Table 42 — Feedback loop mechanical dimensions

TL0		TL1	TL2	TL3	R	C
Min	Max					
12.4	12.6	2.5	0.6	1.0	equals R_{TERM} of Yn/ Yn#	0 pF typ[1]

1. Pads should be present as parasitics are part of the feedback loop. If pads are not present feedback loop length must be corrected.

Exhibit 63

6　　　Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*

JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*

JESD21-C, *Configuration for Solid State Memories.*

JESD8-11A, *Definition of wide range non-terminated logic*

Exhibit 63

Standard Improvement Form   **JEDEC** _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC   Fax: 703.907.7583
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

1. I recommend changes to the following:
    ☐   Requirement, clause number   _____

    ☐   Test method number   _____   Clause number   _____

        The referenced clause number has proven to be:
    ☐   Unclear   ☐   Too Rigid   ☐   In Error

    ☐   Other   _____

2. Recommendations for correction:
    _____
    _____
    _____
    _____

3. Other suggestions for document improvement:
    _____
    _____
    _____
    _____

Submitted by

Name: _____   Phone: _____

Company: _____   E-mail: _____

Address: _____

City/State/Zip: _____   Date: _____

Rev. 9/02

Exhibit 63

Exhibit 63

EXHIBIT O

JEDEC STANDARD

**Definition of the
SSTE32882 Registering Clock Driver
with Parity and Quad Chip Selects for
DDR3 RDIMM 1.25V Applications**

**JESDxx-x
Item #XXX**

Proposal

May 2009

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Exhibit 64

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7559 or www.jedec.org.

Published by

Price: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering
Documents, USA and Canada (1-800-854-7179), International (303-397-7956)

Exhibit 64

PLEASE!

DON'T VIOLATE
THE
LAW!
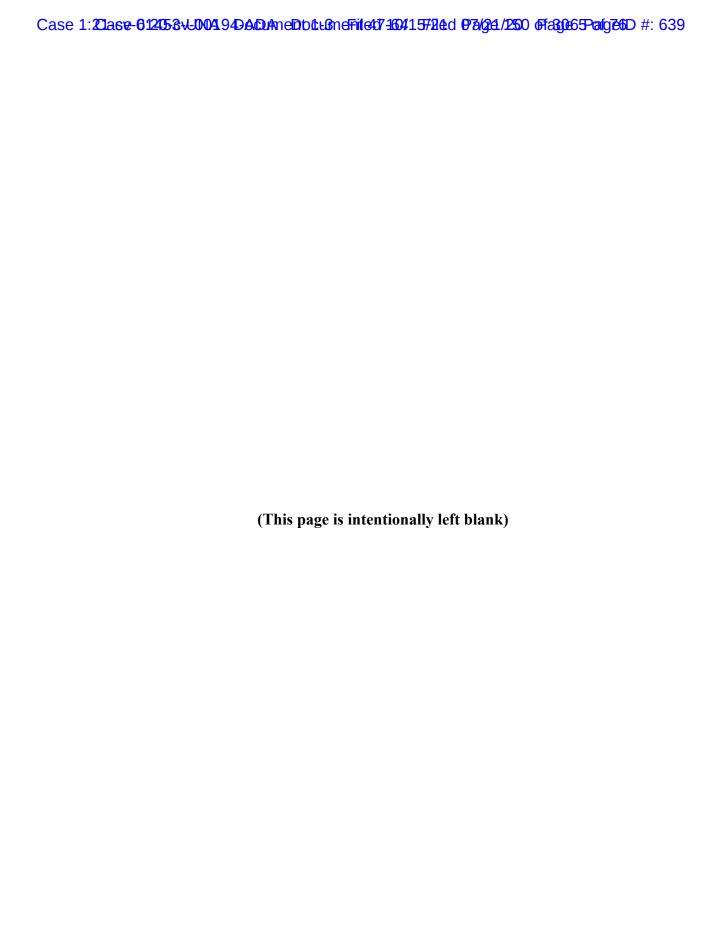
This document is copyrighted by the JEDEC Solid State Technology Association
and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies
through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

Exhibit 64

(This page is intentionally left blank)

Exhibit 64

Case 1:Case 612-cv-00194-DADAmenDociumerit 64-15 Filed 07/21/251 6/age66PagaD #: 640
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 1

DEFINITION OF THE SSTE32882 REGISTERING CLOCK DRIVER WITH PARITY AND QUAD CHIP SELECTS FOR DDR3 RDIMM 1.25V APPLICATIONS

(From JEDEC Board Ballot JCB-03-xx, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

---

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTE32882 registered buffer with parity for driving address and control nets on DDR3 RDIMM applications.

The purpose is to provide a standard for the SSTE32882 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE   The designation SSTE32882 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

---

2 Device standard

2.1 Description

This 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for 1.25V V_{DD} operation.

All inputs are 1.25V CMOS compatible. All outputs are 1.25V CMOS drivers optimized to drive single terminated 25..50 Ohms traces in DDR3 RDIMM applications. The clock outputs Yn and Yn# and control net outputs QnCKEn, QnCSn# and QnODTn can be driven with a different strength and skew to compensate for different loading and equalize signal travel speed.

The SSTE32882 has two basic modes of operation associated with the Quad Chip Select Enable (QCSEN#) input. When the QCSEN# input pin is open (or pulled HIGH), the component has two chip select inputs, DCS0# and DCS1#, and two copies of each chip select output, QACS0#, QACS1#, QBCS0# and QBCS1#. This is the "QuadCS disabled" mode. When the QCSEN# input pin is pulled LOW, the component has four chip select inputs DCS[3:0]#, and four chip select outputs, QCS[3:0]#. This is the "QuadCS enabled" mode. Through the remainder of this specification, DCS[n:0]# will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. QxCS[n:0]# will indicate all of the chip select outputs.

The SSTE32882 operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going HIGH, and CK# going LOW. The data could be either re-driven to the outputs once exactly one of the input signals DCS[n:0]# is driven LOW or it could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in chapter 2.2.

Based on control register settings the device can change its output characteristics to match different DIMM net topologies. The timing can be changed to compensate for different flight time of signals within the target application. By disabling unused outputs the power consumption is reduced.

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 2

2.1.1 Initialization

The LV (Low Voltage) SSTE32882 can be powered-on at 1.25V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET# asserted. When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. Therefore the reference voltage (V_{REF}) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE0, QACKE1, QBCKE0 and QBCKE1 must drive LOW during reset. All other outputs must float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW. After reset and after the stabilization time (t_{STAB}) the register must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3 RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two.

Figure 1 — Timing of clock and data during initialization sequence

(1) CK# is left out for better visibility

(2) DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range

(3) QxCKEn, QxODTn, QxCSn# are not included in this range.

(4) n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode

Exhibit 64

From a device perspective, the initialization sequence must be as shown in Table 1.

Table 1 — SSTE32882 Device Initialization Sequence[1]

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device						
	VDD, AVDD, PVDD	RESET#	Vref	DCS#[n:0][2]	DODT[0:1]	DCKE[0:1]	DA/C	PAR_IN	CK CK#	QCS#[n:0][2]	QODT[0:1]	QCKE[0:1]	QxA/C	ERR OUT#	Y[0:3] Y#[0:3]	FB OUT[3]
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z	Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2[4]	V_{DD} 1.25V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L[5]	Z	H[5]	Z	Z
3	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
4	V_{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[6]	L	X	H	running	running
7[7]	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).						

1. X = Logic LOW or logic HIGH. Z = floating.
2. n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode
3. The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.
4. The system may power up using 1.25V. The BIOS reads the SPD and adjusts the voltage if needed. Stable power is provided for a minimum of 200 uS with RESET# asserted.
5. QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.25V (nominal).
6. This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within ($t_{STAB} - t_{ACT}$) us, the state of QxODTx is a function of DODTx (HIGH or LOW).
7. Step 7 is a typical usage example and is not a register requirement.

As part of the initialization all control words are reset to their default state which is "0", except for RC6 and RC7, which are vendor-defined. After initialization, the memory controller does only need to write to those control registers whose contents need to be changed.

2.1.1.1 Reset Initialization with Stable Power

The timing diagram in Figure 1 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# will be asserted for minimum 100ns. This RESET# timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3 Specification.

Exhibit 64

Case 1:Case-12v53v-004194DADAmeDn1.uGnerFilet47:1641-571ed Pa/ge1/254 6F3age9 Pa0fge6D #: 643
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 4

Figure 2 — Timing of clock and data during initialization sequence with stable power

(1) CK# left out for better visibility

(2) DCKE0, DCKE1, DODT0, DODT1, DCS0# and DCS1# are not included in this range

(3) QxCKEn, QxODTn, QxCSn# are not included in this range.

(4) n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.

Table 2 — SSTE32882 Device Initialization Sequence[1] when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller							Outputs: Signals provided by the device						
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:1][2]	DODT [0:1]	DCKE [0:1]	DA/C	PAR_IN	CK CK#	QCS# [0:1]	QODT [0:1]	QCKE [0:1]	QxA/C	ERR OUT#	Y[0:3] Y#[0:3]	FB OUT[3]
0	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
1	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
2	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L[4]	Z	H[4]	Z	Z
3	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z	Z
4	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[5]	L	X	H	running	running
7	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).						

1.X = Logic LOW or logic HIGH. Z = floating.

PASS-HOLD

Exhibit 64

2.n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode

3.The feedback clock (FBOUT and FBOUT#) pins may or may not be actively driven by the device.

4.QxCKEn and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and V_{DD} is nominal.

5. This indicates the state of QxODTx after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}) us, the state of QxODTx is a function of DODTx (HIGH or LOW).

2.1.2 Parity

The SSTE32882 includes a parity checking function. The SSTE32882 accepts a parity bit from the memory controller at its input pin PAR_IN one cycle after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain ERROUT# pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]# signals being LOW.

If an error occurs, and ERROUT# is driven LOW with the third input clock edge after the corresponding data on the D-inputs. It becomes high impedance with the 5th input clock cycle after the data corresponding with a parity error. In case of consecutive errors ERROUT# becomes high impedance with the 5th input clock cycle after the last data corresponding with a parity error. The DIMM-dependent signals (DCKE0, DCKE1, DCS0#, DCS1#, DODT0 and DODT1) are not included in the parity check computations.

2.1.2.1 Parity Timing Scheme Waveforms

The PAR_IN signal arrives one input clock cycle after the corresponding data input signals. ERROUT# is generated three input clock cycles after the corresponding data is registered. If ERROUT# goes LOW, it stays LOW for a minimum of two input clock cycles or until RESET# is driven LOW. Figure 3 shows the parity diagram with single parity-error occurrence and assumes the occurrence of only one parity error when data is clocked in at the n input clock cycle (PAR_IN clocked in on the n+1 input clock cycle).

Figure 3 — Timing of clock, data and parity signals

(1) CK# left out for better visibility

Figure 4 shows the parity diagram with two consecutive parity-error occurrences and assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles).

Exhibit 64

Figure 4 — Two Consecutive Parity-Error Occurrences

ERROUT# resulting from CA0 - P0, followed by 2nd error in CA1 - P1

(1) CK# left out for better visibility

Figure 5 shows the parity diagram with two parity-error occurrences separated by a clock cycle with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+2 input clock cycles (PAR_IN clocked in on the n+1 and n+3 input clock cycles).

Figure 5 — Two Parity-Error Occurrences Separated by a Clock Cycle of no Error Occurrence

ERROUT# resulting from CA0 - P0, followed by 2nd error in CA2 - P2

(1) CK# left out for better visibility

Figure 6 shows the parity diagram with two parity-error occurrences separated by two input clock cycles with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles).

Figure 6 — Two Parity-Error Occurrences Separated by two Clock Cycle of no Error Occurrence

ERROUT# resulting from CA0 - P0, followed by 2nd error in CA3 - P3

(1) CK# left out for better visibility

Figure 7 shows the parity diagram with two parity-error occurrences; during chip-select and chip-deselect modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles). Parity error in the chip-select mode is detected, but parity error in the chip-deselect mode is ignored.

PASS-HOLD

Exhibit 64

PASS-HOLD

Figure 7 — Parity-Error Occurrence In Chip-Deselect Mode

(1) CK# left out for better visibility

Figure 8 shows the parity diagram with two parity-error occurrences; during normal operation and during control register programming. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles). The data on the n+3 input clock pulse is intended for the control mode register. Parity error during control mode register programming is detected and the parity functionality is the same as during normal operation. If a parity error occurs, the command is ignored.

Figure 8 — Parity-Error Occurrences During Control Word Programming

(1) CK# left out for better visibility

2.1.3 Power saving modes

The device supports different power saving mechanisms.

When both inputs CK and CK# are being held LOW the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1 which are kept driven LOW. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs DCS[n:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW for a certain period of time (t_{ACT}). The input clock must be stable for a time (t_{STAB}) before any access to the device takes place. Stopping the clocks (CK=CK#=LOW) will only put the SSTE32882 in the low-power mode and will not clear the content of the Control Words. The command mode registers will reset only when RESET# is driven LOW.

A float feature can be enabled by setting the corresponding bit in the control register. This causes the device to monitor all the DCS[n:0]# inputs and to float all outputs corresponding with the chip select gated

Exhibit 64

inputs when all the DCS[n:0]# inputs are HIGH. If any one of the DCS[n:0]# input is LOW, the Qn outputs will function normally.

Once all the DCS[n:0]# inputs are HIGH, the gated address command inputs to the register can float to conserve input termination power. DCKE0, DCKE1, DODT0 and DODT1 need to be driven by the system all the time.

The RESET# input has priority over all other power saving mechanisms. When RESET# is driven LOW, it will force the Qn outputs to float, the ERROUT# output HIGH, the QACKE0, QACKE1, QBCKE0 and QBCKE1 outputs LOW and disables Input Bus Termination (IBT).

2.1.4 Register CKE Power Down

The SSTE32882 monitors both DCKEn input signals and enters into power saving state when it latches LOW on both DCKEn inputs and at least one of the DCKEn input has transitioned from HIGH to LOW. If either input Chip Select signal, DCS[n:0]#, is asserted together with DCKEn, the SSTE32882 transfers the corresponding command to its outputs together with QxCKEn LOW.

There are two modes of CKE Power Down selected by control word RC9. Bit DBA0 in RC9 indicates whether register turns off IBT or keeps IBT on.

2.1.4.1 Register CKE Power Down with IBT Off

Upon entry into CKE Power Down mode with IBT off, all register input buffers including IBT are disabled except for CK/CK#, DCKEn, FBIN, FBIN# and RESET#. The SSTE32882 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK/CK#, DCKEn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxODTn and QxCKEn outputs are driven LOW. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 9.

Exhibit 64

Figure 9 — Power Down Mode Entry and Exit with IBT Off

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SSTE32882 into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn input are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the register immediately starts driving HIGH on the appropriate QxCKEn signal. The QxCSn# signals are driven HIGH and QxODTn signals are driven LOW. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all register outputs when QxCKEn goes HIGH. The register drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The register guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 9.

Exhibit 64

2.1.4.2 Register CKE Power Down with IBT On

Upon entry into CKE Power Down Mode with IBT on, all register input buffers excluding IBT are disabled except for CK/CK#, DCKEn, DODTn, FBIN, FBIN# and RESET#. The SSTE32882 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK/CK#, DCKEn, DODTn and RESET#. The SSTE32882 also disables all its output buffers except for Yn/Yn#, QxODTn, QxCKEn and FBOUT/FBOUT#. The Yn/Yn# and FBOUT/FBOUT# outputs continue to drive a valid phase accurate clock signal. The QxCKEn outputs are driven LOW. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 10.

Figure 10 — Power Down Mode Entry and Exit with IBT On

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving DCS[1:0]# LOW is illegal as it will force SSTE32882 into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

To re-enable the SSTE32882 from this Power Down Mode with IBT on, valid logic levels are required at

Exhibit 64

all device inputs when either or both DCKEn inputs are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the SSTE32882 immediately starts driving HIGH on the appropriate QxCKEn signals. The QxCSn# signals are driven HIGH and the QxODTn signals follow the inputs. Other output signals QxRAS#, QxCAS#, QxWE# and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEn goes HIGH. The device drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip select register inputs DCSn# can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn# can be asserted for 1 tCK. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 10.

2.1.5 Clock Stopped Power Down Mode

To support S3 Power Management mode or any other operation that allows Yn clocks to float, the SSTE32882 supports a Clock Stopped power down mode. When both inputs CK and CK# are being held LOW ($V_{IL (static)}$) or float (will eventually settle at LOW because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirement are shown in Figure 11, "Clock Stopped Power Down Entry and Exit with IBT On" and Figure 12, "Clock Stopped Power Down Entry and Exit with IBT Off". The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1, which must be kept driven LOW. The Clock Stopped power down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all register outputs besides QxCKE0 and QxCKE1 can be disabled.

Clock Stopped Power Down Mode Entry

To enter Clock Stopped Power Down mode, the register will first enter CKE power down mode. Once in CKE power down mode, DCKEn will continue be deasserted for a minimum of one tCKoff before pulling CK and CK# LOW. After holding CK and CK# LOW ($V_{IL (static)}$) for at least one tCKEV, both CK and CK# can be floated (because of the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer, CK/CK# will stay at LOW even though they are not being driven). The register is now in Clock Stopped Power Down mode. After CK and CK# are pulled LOW, DCKEn will remain LOW for at least one tCKEV before it can floated (if needed to be float). At this point, all input receivers and input termination of the SSTE32882 are disabled. The only active input circuits are CK and CK#, which are required to detect the wake up request from the host.

Clock Stopped Power Down Mode Exit

To wake up the register after entering Clock Stopped Power Down, the register inputs DCS[n:0]# must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, a frequency and phase accurate input clock signal must be applied. Within tACT after CK and CK# resumed normal operation, the SSTE32882 outputs start becoming a function of their corresponding inputs. The state of the DCS[n:0]# inputs must not be changed before the end of tSTAB. The input clock CK and CK# must be stable for a time equal or greater than tSTAB before any access to the SSTE32882 can take place.

Exhibit 64

PASS-HOLD

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 12

Figure 11 — Clock Stopped Power Down Entry and Exit with IBT On

PASS-HOLD

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) With RC9 DBA0='0'
(3) When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.
(4) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn#
    outputs will follow DCSn# inputs.

Exhibit 64

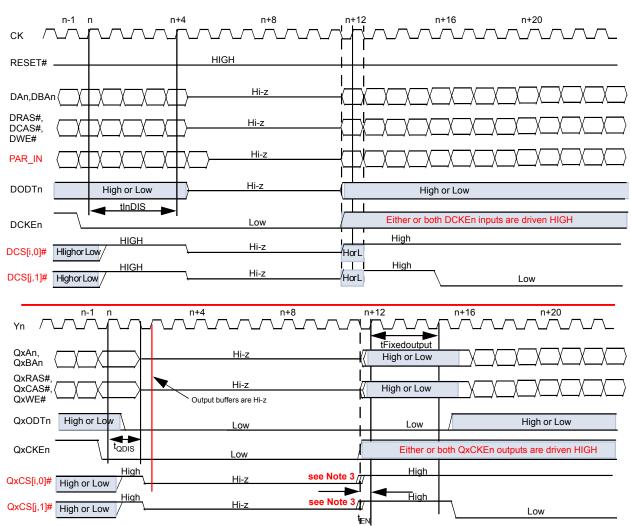**Figure 12 — Clock Stopped Power Down Entry and Exit with IBT Off**

(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3
(2) With RC9 DBA0='1'
(3) When CK/CK# inputs are floated, CK/CK# inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/CK# input buffer.
(4) Upon CKE Power Down exit, QxCSn# will be held HIGH for maximum of 1 tCK regardless of what DCSn# input level is. For all other operation QxCSn# outputs will follow DCSn# inputs.

Exhibit 64

2.1.6 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling

Output Inversion is always enabled by default, after RESET# is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs, however the following B-outputs will be driven to the complement of the matching A-outputs: QBA3 - QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2.

Figure 13 — Output Inversion Functional Diagram

The Output Inversion feature is not used during DRAM MRS command access. When Output Inversion is disabled, all corresponding A and B output drivers of the SSTE32882 are driven to the same logic levels. Output Inversion must be disabled when the MRS and EMRS commands must be issued to the DRAMs, for example, to assure that the same programming is issued to all DRAMs in a rank.

With Output Inversion disabled during MRS access, in order to allow correct DRAM accesses with the consequently increased simultaneous switching propagation delay the devices supports 3T timing. If this feature is invoked the device drives the received data on its outputs for thee cycles instead of one. The only exception are the QxCS[n:0]# outputs, which are the QACS0#, QACS1#, QBCS0# and QBCS1# outputs in the QuadCS disabled mode and are QCS[3:0]# in the QuadCS enabled mode.

When the device decodes the MRS command (DRAS#=0, DCAS#=0, DWE=0 and only one DCSn#=0), it will disable the Output Inversion function and pass the DRAM MRS command with an additional (one) clock delay on the appropriate QnCSx# signal to the DRAM. Back-to-back MRS command via the SSTE32882 must have a minimum of three clock delays. The SSTE32882 will automatically enable Output Inversion if there is no DRAM MRS command three clocks after the previous MRS command.

The inputs and outputs relationships for 1T timing and 3T timing are shown in Figure 14, Figure 15 and Figure 16.

Exhibit 64

Figure 14 — 1T Timing During Normal Operation

(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

PASS-HOLD

Exhibit 64

Figure 15 — 3T Timing During DRAM MRS Command

(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Exhibit 64

Figure 16 — 3T Timing During Multiple DRAM MRS Commands

(1) CK# and Yn# left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

PASS-HOLD

Exhibit 64

PASS-HOLD

2.2 Control words

The SSTE32882 registers have internal control bits for adapting the configuration of certain device features. The control bits are accessed by the simultaneous assertion of both DCS0# and DCS1# in the QuadCS disabled mode. In the QuadCS enable mode, the simultaneous assertion of both DCS2# and DCS3# during normal operation, and the assertion of all four DCS[3:0]# inputs also result in control word access. However, assertion of any three DCS[3:0]# inputs is not legal. Register Qn outputs including QxCKE0, QxCKE1, QxODT0 and QxODT1 remain in their previous state. Select signals QxCS[n:0]# are set to HIGH during control word access.

The SSTE32882 allocates decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0 and DBA1. Bits DA[15:5] must be LOW and at least one DCKEn input must be HIGH for a valid access. During control word write, at least one DCKEn must be asserted. If register CKE power down feature is disabled, DCKEn input is a don't care (either HIGH or LOW). The inputs on DRAS#, DCAS#, DWE# and DODT[1:0] can be either HIGH or LOW and are ignored by the register during control word access. In all cases Address and command parity is checked during control word write operations. ERROUT# is asserted and the command is ignored if a parity error is detected. Using this mechanism, controllers may use the SSTE32882 to validate the address and command bus signal integrity to the module as long as one or more of the parity checked input signals DA3..DA15, DBA0, DBA1, DRAS#, DCAS#, DWE# are kept HIGH.

Control word access must be possible at any defined frequency independent of the current setting of RC2[DBA1] control registers.

Exhibit 64

2.3 Pinout configuration

Package options includes 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 11 x 20 grid, 8.0mm x 13.5mm. It is using the mechanical outline MO-246 variation F. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

Figure 17 — Pinout Configuration

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 20

2.3.1 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode disabled)

176-ball, 11 · 20 grid, TOP VIEW

Table 3, "Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

Table 3 — Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD		VDD	VDD	VDD		VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD		VDD	VDD	VDD		VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS#
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DODT1
T	DCKE0	DCS0#								DCS1#	DODT0
U	DA12	DBA2		Y1#	PVSS	VDD	PVDD	Y0#		DA13	DCAS#
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		DRAS#	DWE#
W	DA8	DA6	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions -- must not be connected on system
Pins Y2 and R6 are reserved for DCS2# and DCS3# in the QuadCS mode and must not be connected on system, the device design needs to tolerate this floating pin
Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

Exhibit 64

2.3.2 Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode disabled)

Table 4, "Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in back configuration with QuadCS mode disabled.

Table 4 — Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD		VDD	VDD	VDD		VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD		VDD	VDD	VDD		VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	QBRAS#
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	DCS1#								DCS0#	DCKE0
U	DCAS#	DA13		Y1#	PVSS	VDD	PVDD	Y0#		DBA2	DA12
V	DWE#	DRAS#		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	RSVD	DA7

Pins A9 and W7 are reserved for future functions -- must not be connected on system
Pin Y10 and R6 are reserved for DCS2# and DCS3# in the QuadCS mode and must not be connected on system, the device design needs to tolerate this floating pin
Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

PASS-HOLD

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 22

2.3.3 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode enabled)

Table 5, "Ball Assignment; MIRROR=LOW, QCSEN#=LOW," specifies the pinout for SSTE32882 in front configuration with QuadCS mode enabled.

Table 5 — Ball Assignment; MIRROR=LOW, QCSEN#=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD		VDD	VDD	VDD		VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD		VDD	VDD	VDD		VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS#
R	DCKE1	DA14	DA15		DA5	DCS3#	DA2		DA1	DA10	DODT1
T	DCKE0	DCS0#								DCS1#	DODT0
U	DA12	DBA2		Y1#	PVSS	VDD	PVDD	Y0#		DA13	DCAS#
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		DRAS#	DWE#
W	DA8	DA6	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA0	DBA0
Y	DA7	DCS2#	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions -- must not be connected on system

Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

PASS-HOLD

Exhibit 64

2.3.4 Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode enabled)

Table 6, "Ball Assignment; MIRROR=HIGH, QCSEN#=LOW," specifies the pinout for SSTE32882 in back configuration with QuadCS mode enabled.

Table 6 — Ball Assignment; MIRROR=HIGH, QCSEN#=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	QCSEN#	VSS	RESET#	MIRROR	ERROUT#	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD		VDD	VDD	VDD		VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD		VDD	VDD	VDD		VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	QBRAS#
R	DODT1	DA10	DA1		DA2	DCS3#	DA5		DA15	DA14	DCKE1
T	DODT0	DCS1#								DCS0#	DCKE0
U	DCAS#	DA13		Y1#	PVSS	VDD	PVDD	Y0#		DBA2	DA12
V	DWE#	DRAS#		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	FBIN#	Y3#	AVSS	CK#	RSVD	Y2#	FBOUT#	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	DCS2#	DA7

Pins A9 and W7 are reserved for future functions -- must not be connected on system
Blank space indicate no ball is populated at that gridpoint -- vias on the module may be located in these areas

PASS-HOLD

Exhibit 64

2.4 Pinout configuration narrow package[1]

Optional the device is available as 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 8 x 22 grid, 6.0mm x 15mm. It is using the mechanical outline MO-246 variation B. Equivalent to the 11 x 20 grid configuration the device pinout supports outputs on the outer two left and right columns. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias.

Figure 18 — Pinout Configuration

1. This package may only be used in new DIMM designs. It is not intended for use in the existing DIMM's.

Exhibit 64

2.4.1 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode disabled)

176-ball, 8 x 22 grid, TOP VIEW

Table 7, "Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in front configuration with QuadCS mode disabled. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

Table 7 — Ball Assignment; MIRROR=LOW, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD	VDD	VDD	VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD	VDD	VDD	VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	DCS0#	DCKE0	VSS	VSS	VSS	VSS	DODT0	DCS1#
U	DA12	DA3	Y1#	PVSS	PVDD	Y0#	DA4	DCAS#
V	DA5	DA9	Y1	PVSS	PVDD	Y0	DWE#	DA2
W	DA8	DA15	Y3#	PVSS	PVDD	Y2#	DA1	DBA0
Y	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	RSVD	FBIN#	CK#	RSVD	FBOUT#	PAR_IN	DRAS#
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA0

Pins A6, AA2, AA5, AB2 and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Exhibit 64

PASS-HOLD

2.4.2 Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode disabled)

Table 8, "Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)," specifies the pinout for SSTE32882 in back configuration with QuadCS mode disabled.

Table 8 — Ball Assignment; MIRROR=HIGH, QCSEN#=HIGH (or Float)

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QACS1#	VDD	VDD	VDD	VDD	QBCS1#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QACS0#	VDD	VDD	VDD	VDD	QBCS0#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	DCS1#	DODT0	VSS	VSS	VSS	VSS	DCKE0	DCS0#
U	DCAS#	DA4	Y1#	PVSS	PVDD	Y0#	DA3	DA12
V	DA2	DWE#	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	Y3#	PVSS	PVDD	Y2#	DA15	DA8
Y	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	DRAS#	PAR_IN	FBIN#	CK#	RSVD	FBOUT#	RSVD	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	RSVD	DA6

Pins A6, AA5, AA7, AB2 and AB7 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Exhibit 64

Case 1:23-cv-01203-UNA Document 1-3 Filed 04/15/21 Page 177 of 306 PageID #: 666
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 27

2.4.3 Pinout top view for 176-ball TFBGA (front configuration, QuadCS mode enabled)

Table 9, "Ball Assignment; MIRROR=LOW, QCSEN#=LOW," specifies the pinout for SSTE32882 in front configuration with QuadCS mode enabled.

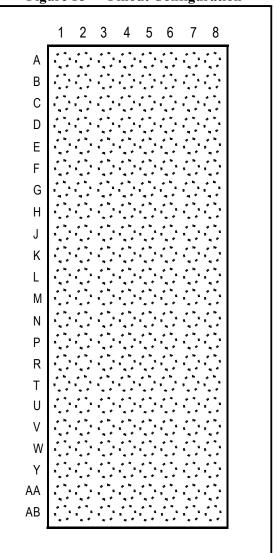**Table 9 — Ball Assignment; MIRROR=LOW, QCSEN#=LOW**

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD	VDD	VDD	VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD	VDD	VDD	VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA14	DCKE1	VDD	VDD	VDD	VDD	DODT1	DA10
T	DCS0#	DCKE0	VSS	VSS	VSS	VSS	DODT0	DCS1#
U	DA12	DA3	Y1#	PVSS	PVDD	Y0#	DA4	DCAS#
V	DA5	DA9	Y1	PVSS	PVDD	Y0	DWE#	DA2
W	DA8	DA15	Y3#	PVSS	PVDD	Y2#	DA1	DBA0
Y	DA7	DBA2	Y3	AVSS	AVDD	Y2	DA13	DBA1
AA	DA11	DCS2#	FBIN#	CK#	RSVD	FBOUT#	PAR_IN	DRAS#
AB	DA6	RSVD	FBIN	CK	VREFCA	FBOUT	DCS3#	DA0

Pins A6, AA5 and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 28

2.4.4 Pinout top view for 176-ball TFBGA (back configuration, QuadCS mode enabled)

Table 10, "Ball Assignment; MIRROR=HIGH, QCSEN#=LOW)," specifies the pinout for SSTE32882 in back configuration with QuadCS mode enabled.

Table 10 — Ball Assignment; MIRROR=HIGH, QCSEN#=LOW)

	1	2	3	4	5	6	7	8
A	QAA13	QAA8	QCSEN#	RESET#	ERROUT#	RSVD	QBA8	QBA13
B	QAA14	QAA7	VSS	VSS	MIRROR	VSS	QBA7	QBA14
C	QAA9	QAA6	VDD	VDD	VDD	VDD	QBA6	QBA9
D	QAA11	QAA5	VSS	VSS	VSS	VSS	QBA5	QBA11
E	QAA2	QAA4	VDD	VDD	VDD	VDD	QBA4	QBA2
F	QAA1	QAA3	VSS	VSS	VSS	VSS	QBA3	QBA1
G	QAA0	QABA1	VDD	VDD	VDD	VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS	VSS	VSS	VSS	QBBA0	QBA12
J	QABA2	QCS1#	VDD	VDD	VDD	VDD	QCS3#	QBBA2
K	QAA15	QACKE0	VSS	VSS	VSS	VSS	QBCKE0	QBA15
L	QAWE#	QCS0#	VDD	VDD	VDD	VDD	QCS2#	QBWE#
M	QAA10	QACKE1	VSS	VSS	VSS	VSS	QBCKE1	QBA10
N	QACAS#	QAODT0	VDD	VDD	VDD	VDD	QBODT0	QBCAS#
P	QARAS#	QAODT1	VSS	VSS	VSS	VSS	QBODT1	QBRAS#
R	DA10	DODT1	VDD	VDD	VDD	VDD	DCKE1	DA14
T	DCS1#	DODT0	VSS	VSS	VSS	VSS	DCKE0	DCS0#
U	DCAS#	DA4	Y1#	PVSS	PVDD	Y0#	DA3	DA12
V	DA2	DWE#	Y1	PVSS	PVDD	Y0	DA9	DA5
W	DBA0	DA1	Y3#	PVSS	PVDD	Y2#	DA15	DA8
Y	DBA1	DA13	Y3	AVSS	AVDD	Y2	DBA2	DA7
AA	DRAS#	PAR_IN	FBIN#	CK#	RSVD	FBOUT#	DCS2#	DA11
AB	DA0	RSVD	FBIN	CK	VREFCA	FBOUT	DCS3#	DA6

Pins A6, AA5 and AB2 are reserved for future functions must not be connected on system. The system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Exhibit 64

2.5 Terminal Functions

Table 11 — Terminal functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE0/1, DODT0/1	1.25V CMOS Inputs[1]	DRAM corresponding register function pins not associated with Chip Select.
Chip Select gated inputs	DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#	1.25V CMOS Inputs[1]	DRAM corresponding register inputs, re-driven only when either chip select is LOW. If both chip selects are LOW the register maintains the state of the previous input clock cycle at its outputs
Chip Select inputs	DCS0#, DCS1#	1.25V CMOS Inputs[1]	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be LOW when a valid address/command is present which should be re-driven.
	DCS2#, DCS3#	1.25V CMOS Inputs[1]	DRAM corresponding register Chip Select signals when QuadCS mode is enabled. DCS2# and DCS3# inputs are disabled when QuadCS mode is disabled.
Re-driven outputs	QxA0..QxA15, QxBA0..QxBA2, QxCS0/1#, QxCKE0/1, QxODT0/1, QxRAS#, QxCAS#, QxWE#	1.25V CMOS Outputs[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. x is A or B; outputs are grouped as A or B and may be enabled or disabled via RC0.
Parity input	PAR_IN	1.25V CMOS Input[1]	Input parity is received on pin PAR_IN and should maintain parity across the Chip Select Gated inputs (see above), at the rising edge of the input clock, one input clock cycle after corresponding data and one or both chip selects are LOW.
Parity error output	ERROUT#	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. ERROUT# will be active for two clock cycles, and delayed by 3 clock cycles to the corresponding input data
Clock inputs	CK, CK#	1.25V CMOS Inputs[1]	Differential master clock input pair to the PLL; has weak internal pull-down resistors (10K$*$ ~100K$*$).
Clock Outputs	Y0, Y0#.. Y3, Y3#	1.25V CMOS Outputs	Re-driven Clock
Feedback inputs	FBIN, FBIN#	1.25V CMOS Inputs[1]	Differential feedback inputs
Feedback outputs	FBOUT, FBOUT#	1.25V CMOS Outputs	Differential feedback outputs
Miscellaneous inputs	RESET#	CMOS[3]	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float. Once RESET# becomes HIGH the outputs get enabled and are driven LOW until the first access has been performed. RESET# also resets the ERROUT# signal.
	MIRROR	CMOS[3]	Selects between two different ballouts for front or back operation. When the MIRROR input is HIGH, the device input bus termination (IBT) is turned off on all inputs, except the DCSn# and DODTn inputs.
	QCSEN#	CMOS[3]	Enables the QuadCS mode. The QCSEN# input has a weak internal pullup resistor (10K$*$ ~100K$*$).
	VREFCA[1]	VDD/2	Input reference voltage for the data inputs.
	VDD	Power Input	Power supply voltage
	VSS	Ground Input	Ground
	AVDD	Analog Power	Analog supply voltage
	AVSS	Analog Ground	Analog ground
	PVDD	Clock Driver Output Power	Clock logic and clock output driver power supply
	PVSS	Clock Driver Output Ground	Clock logic and clock output driver ground
	RSVD	I/O	Reserved pins, must be left floating

1. 1.25V CMOS inputs uses VREFCA as the switching point reference for these receivers.
2. These outputs are optimized for memory applications to drive DRAM inputs to 1.25V signaling levels
3. Voltage levels according standard JESD8-11A, wide range, non terminated logic

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 30

PASS-HOLD

2.6 Function tables

Table 12 — Function table (each flip flop) with QuadCS mode disabled

	Inputs							Outputs				
RESET#	DCS0#	DCS1#	CK[1]	CK#[1]	ADDR[2]	CMD[3]	CTRL[4]	Qn	QxCS0#	QxCS1#	QxODTn	QxCKEn
H	L	L	*	*	Control Word	Control Word	Control Word	No change	H	H	No change	No change
H	X	X	L or H	H or L	X	X	X	No change	No change	No change	No change	No change
H	L	H	*	*	X	X	X	Follows Input	L	H	Follows Input	Follows Input
H	X	X	L	L	X	X	X	Float	Float	Float	Float	L
H	H	L	*	*	X	X	X	Follows Input	H	L	Follows Input	Follows Input
H	H	H	*	*	X or Float	X or Float	X	No change or Float[5]	H	H	Follows Input	Follows Input
L	X or Float	X or Float	X or Float	X or Float	X or Float	X or Float	X or Float	Float	Float	Float	Float	L

1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
2. ADDR = DA[15:0], DBA[2:0]
3. CMD = DRAS#, DCAS#, DWE#
4. CTRL = DODTn, DCKEn
5. Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

Table 13 — Function table (each flip flop) with QuadCS mode enabled

	Inputs				Outputs			
RESET#	DCS[3:0]#	CK[1]	CK#[1]	A/C/E[2]	Qn	QCS[3:0]#	QxODTn	QxCKEn
H	LLHH	*	*	Control Word	No change	HHHH	No change	No change
H	HHLL							
H	LLLL							
H	XXXX	L or H	H or L	X	No change	No change	No change	No change
H	LHHH	*	*	Dn	Dn	LHHH	DODTn	DCKEn
H	HLHH	*	*	Dn	Dn	HLHH	DODTn	DCKEn
H	HHLH	*	*	Dn	Dn	HHLH	DODTn	DCKEn
H	HHHL	*	*	Dn	Dn	HHHL	DODTn	DCKEn
H	LHLH	*	*	Dn	Dn	LHLH	DODTn	DCKEn
H	HLLH	*	*	Dn	Dn	HLLH	DODTn	DCKEn
H	LHHL	*	*	Dn	Dn	LHHL	DODTn	DCKEn
H	HLHL	*	*	Dn	Dn	HLHL	DODTn	DCKEn
H	XXXX	L	L	X	float	float	float	L
H	HHHH	*	*	X	No change or float[3]	HHHH	DODTn	DCKEn
H	LLLH	*	*	X	Ilegal Input States			
H	LLHL							
H	LHLL							
H	HLLL							
L	X or float	X or float	X or float	X or float	float	float	float	L

Exhibit 64

1.It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

2.A/C/E = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, DODTn, DCKEn

3. Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

PASS-HOLD

Table 14 — Parity, LOW power and Standby function table with QuadCS mode disabled

Inputs							Output
RESET#	DCS0#	DCS1#	CK^1	$CK\#^1$	$*$ of A/C^2	PAR_IN^3	ERROUT#^{4}
H	L	X	$*$	$*$	Even	L	H
H	L	X	$*$	$*$	Odd	L	L
H	L	X	$*$	$*$	Even	H	L
H	L	X	$*$	$*$	Odd	H	H
H	X	L	$*$	$*$	Even	L	H
H	X	L	$*$	$*$	Odd	L	L
H	X	L	$*$	$*$	Even	H	L
H	X	L	$*$	$*$	Odd	H	H
H	H	H	$*$	$*$	X	X	H^5
H	X	X	L or H	H or L	X	X	ERROUT#n_0
H	X	X	L	L	X	X	H^6
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

2. A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.

3. PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.

4. This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going LOW. If ERROUT# is LOW, it stays latched LOW for exactly two clock cycles or until RESET# is driven LOW.

5.Same 3 cycle delay for ERROUT# is valid for the de-select phase (see diagram)

6.The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 32

PASS-HOLD

Table 15 — Parity, LOW power and Standby function table with QuadCS mode enabled

	Inputs					Output
RESET#	DCS[3:0]#	CK[1]	CK#[1]	∗ of A/C[2]	PAR_IN[3]	ERROUT#[4]
H	LXXX XLXX XXLX XXXL	∗	∗	Even	L	H
H	LXXX XLXX XXLX XXXL	∗	∗	Odd	L	L
H	LXXX XLXX XXLX XXXL	∗	∗	Even	H	L
H	LXXX XLXX XXLX XXXL	∗	∗	Odd	H	H
H	HHHH	∗	∗	X	X	H[5]
H	XXXX	L or H	H or L	X	X	ERROUT#n_0
H	XXXX	L	L	X	X	H[6]
L	X or floating	X or floating	X or floating	X or floating	X or floating	H

1. It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.

2. A/C = DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#. Inputs DCKE0, DCKE1, DODT0, DODT1, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are not included in this range. This column represents the sum of the number of A/C signals that are electrically HIGH.

3. PAR_IN arrives one clock cycle after data to which it applies, ERROUT# is issued 3 clock cycles after the failing data.

4. This transition assumes ERROUT# is HIGH at the crossing of CK going HIGH and CK# going LOW. If ERROUT# is LOW, it stays latched LOW for exactly two clock cycles or until RESET# is driven LOW.

5. Same 3 cycle delay for ERROUT# is valid for the de-select phase (see diagram)

6. The system is not allowed to pull CK and CK# LOW while ERROUT# is asserted.

Exhibit 64

PASS-HOLD

Table 16 — PLL function table

Inputs					Outputs				
RESET#	AVDD	OEn[1]	CK[2]	CK#[2]	Yn	Yn#	FBOUT	FBOUT#	PLL
L	X	X	X	X	Float	Float	Float	Float	Off
H	V_{DD} nominal	L	L	H	L	H	L	H	On
H	V_{DD} nominal	L	H	L	H	L	H	L	On
H	V_{DD} nominal	H	L	H	Float	Float	L	H	On
H	V_{DD} nominal	H	H	L	Float	Float	H	L	On
H	V_{DD} nominal	X	L	L	Float	Float	Float	Float	Off
H	GND[3]	L	L	H	L	H	L	H	Bypass/Off
H	GND[3]	L	H	L	H	L	H	L	Bypass/Off
H	GND[3]	H	L	H	Float	Float	L	H	Bypass/Off
H	GND[3]	H	H	L	Float	Float	H	L	Bypass/Off
H	GND[3]	X	L	L	Float	Float	Float	Float	Bypass/Off
H	X	X	H	H	Reserved				

1.The Output Enable (OEn) to disable the output buffer is not an input signal to the SSTE32882, but an internal signal from the PLL powerdown control and test logic. It is controlled by setting or clearing the corresponding bit in the Clock Driver mode register.
2.It is illegal to hold both the CK and CK# inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when RESET# is driven HIGH.
3.This is a device test mode and all register timing parameter are not guaranteed.

Exhibit 64

2.7 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RC2 (bit DBA1 and DA3) and RC10, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC2: bit DBA1 and DA3, and RC10) this settling may take up to t_{STAB} time. All chip select inputs, DCS[n:0]#, must be kept HIGH during that time. The Control Words can be accessed and written to when running within any one defined frequency band.

2.7.1 Control Word Decoding

The values to be programmed into each control word are presented on signals DA3, DA4, DBA0 and DBA1 simultaneously with the assertion of the control word access through DCS0# and DCS1#, or DCS2# and DCS3# in the QuadCS enabled mode, and the address of the control word on DA0, DA1, DA2 and DBA2.

The reset default state of Control Words 0 .. 5 and Control Words 8 .. 15 is "0". The reset default state for Control Words 6 and 7 is Vendor Specific. Every time the device is reset, its default state is restored. Stopping the clocks (CK=CK#=LOW) to put the device in low-power mode will not alter the control word settings.

Table 17 — Control Word Decoding with QuadCS mode disabled

Control Word	Symbol	Signal						Meaning
		DCS0#	DCS1#	DBA2	DA2	DA1	DA0	
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Global Features Control word
Control word 1	RC1	L	L	L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2	L	L	L	L	H	L	Timing Control word
Control word 3	RC3	L	L	L	L	H	H	CA Signals Driver Characteristics Control word
Control word 4	RC4	L	L	L	H	L	L	Control Signals Driver Characteristics Control word
Control word 5	RC5	L	L	L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6	L	L	L	H	H	L	Reserved, free to use by vendor
Control word 7	RC7	L	L	L	H	H	H	Reserved, free to use by vendor
Control word 8	RC8	L	L	H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9	L	L	H	L	L	H	Power Saving Settings Control Word
Control word 10	RC10	L	L	H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11	L	L	H	L	H	H	Encoding for RDIMM Operating V_{DD}
Control word 12	RC12	L	L	H	H	L	L	Reserved for future use
Control word 13	RC13	L	L	H	H	L	H	Reserved for future use
Control word 14	RC14	L	L	H	H	H	L	Reserved for future use
Control word 15	RC15	L	L	H	H	H	H	Reserved for future use

Exhibit 64

Table 18 — Control Word Decoding with QuadCS mode enabled

Control Word	Symbol	DCS[3:0]#	DBA2	DA2	DA1	DA0	Meaning
		Signal					
None	n/a	HXHX	X	X	X	X	No control word access
None	n/a	HXXH	X	X	X	X	
None	n/a	XHHX	X	X	X	X	
None	n/a	XHXH	X	X	X	X	
None	n/a	HLLL	X	X	X	X	Ilegal Input States
None	n/a	LHLL	X	X	X	X	
None	n/a	LLHL	X	X	X	X	
None	n/a	LLLH	X	X	X	X	
Control word 0	RC0	LLHH or HHLL or LLLL	L	L	L	L	Global Features Control word
Control word 1	RC1		L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2		L	L	H	L	Timing Control word
Control word 3	RC3		L	L	H	H	CA Signals Driver Characteristics Control word
Control word 4	RC4		L	H	L	L	Control Signals Driver Characteristics Control word
Control word 5	RC5		L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6		L	H	H	L	Reserved, free to use by vendor
Control word 7	RC7		L	H	H	H	Reserved, free to use by vendor
Control word 8	RC8		H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9		H	L	L	H	Power Saving Settings Control Word
Control word 10	RC10		H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11		H	L	H	H	Encoding for RDIMM Operating V_{DD}
Control word 12	RC12		H	H	L	L	Reserved for future use
Control word 13	RC13		H	H	L	H	Reserved for future use
Control word 14	RC14		H	H	H	L	Reserved for future use
Control word 15	RC15		H	H	H	H	Reserved for future use

PASS-HOLD

Exhibit 64

2.7.2 Control Word Functions

The following sections describe the contents of each control word.

Table 19 — RC0: Global Features Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Output Inversion	Output Inversion enabled
x	x	x	1		Output Inversion disabled
x	x	0	x	Floating Outputs (when DCSn# = HIGH, and DA4 = "1")	Float disabled (normal output drive strength as defined in RC3, 4, and 5)
x	x	1	x		Float enabled (or Weak Drive mode when RC9 [DA3=1])
x	0	x	x	A outputs disabled	A outputs enabled
x	1	x	x		A outputs disabled
0	x	x	x	B outputs disabled	B outputs enabled
1	x	x	x		B outputs disabled

Output floating refers to allowing many A/B outputs to enter a hi-Z state when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g., VDD, VTT, or VSS). When output floating is enabled, the following outputs (on both matching A and B outputs) are hi-Z when not actively driven: QxA0, QxA1, QxA2, QxA3, QxA4, QxA5, QxA6, QxA7, QxA8, QxA9, QxA10/AP, QxA11, QxA12/BC, QxA13, QxA14, QxA15, QxBA0, QxBA1, QxBA2, QxRAS#, QxCAS#, and QxWE#.

A or B output disable allows the use of the SSTE32882 in reduced parts count applications such as DDR3 Mini-RDIMMs. When output disable is asserted, all outputs on the corresponding side of the register including the clock drivers remain in Hi-Z at all times.

Table 20 — RC1: Clock Driver Enable Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Disable Y0/Y0# clock	Y0/Y0# clock enabled
x	x	x	1		Y0/Y0# clock disabled
x	x	0	x	Disable Y1/Y1# clock	Y1/Y1# clock enabled
x	x	1	x		Y1/Y1# clock disabled
x	0	x	x	Disable Y2/Y2# clock	Y2/Y2# clock enabled
x	1	x	x		Y2/Y2# clock disabled
0	x	x	x	Disable Y3/Y3# clock	Y3/Y3# clock enabled
1	x	x	x		Y3/Y3# clock disabled

Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on CK/CK#

Exhibit 64

Case 1:23-cv-01453-UNA Document 1-3 Filed 04/15/21 Page 187 of 306 PageID #: 676
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 37

unless the system stops the clock inputs to the SSTE32882 to enter the lowest power mode.

Table 21 — RC2: Timing Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Address- and command-nets pre-launch (Control Signals QxCKE, QxCS, QxODT do not apply)	Standard (1/2 Clock)
x	x	x	1		Address and command nets pre-launch (3/4 Clock)
x	x	0	x	1T/3T Output timing	1T timing
x	x	1	x		3T timing[1]
x	0	x	x	Input Bus Termination[2]	100 Ohm
x	1	x	x		150 Ohm
0	x	x	x	Frequency Band Select	Operation (Frequency Band 1)
1	x	x	x		Test Mode (Frequency Band 2)

1.There is no floating once 3T timing is activated.
2.If MIRROR is 'HIGH' then Input Bus Termination (IBT) is turned off on all inputs, except the DCSn# and DODTn inputs.

The Input Bus Termination (IBT) is also located in this control word with two options of 100 Ohms or 150 Ohms which can be selected to adapt to different system scenarios. At power-up, the SSTE32882 IBT defaults to 100 Ohms. The system controller can reprogram the termination resistance to 150 Ohms by setting this bit. Only the DAn, DBAn, DRAS#, DCAS#, DWE#, DCSn#, DODT, DCKEn and PAR_IN inputs have the IBT. The CK, CK#, FBIN, FBIN#, RESET# and MIRROR inputs do not have IBT.

If MIRROR is 'HIGH' then it is assumed the register is located on the back side of a module where two registers are tied together on the input side. In this case, for the register on the back side, IBT are turned off on all inputs, except the DCSn# and DODTn inputs.

The following diagram illustrates the pre-launch feature whereby double loaded nets in a 2-rank configuration can be driven with an earlier signal compared to output clock and control in order to compensate for the slower signal travel speed. This timing applies at all supported frequencies.

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
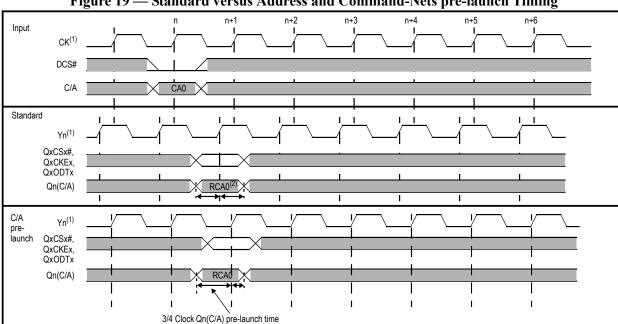Page 38

Figure 19 — Standard versus Address and Command-Nets pre-launch Timing

PASS-HOLD

(1) CK# and Yn# left out for better visibility
(2) RCA0 is re-driven command address signal based on input CA0

1. DCS[n:0]# indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled.
   QxCS[n:0] indicates all of the chip select outputs.

Exhibit 64

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals =QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#
- Control Signals = QxCSn#, QxCKEn, QxODTn
- CK = Yn .. Yn#

2.8 Register Output Slew-Rate & R-on Targets for Each Drive Strength

Table 22 — Output Slew-Rate & R-on Targets

Drive Settings	Output Driver R-on Targets (Ohms)			Output Slew-Rate (V/ns)					
				Range (1.25V) DDR3U-800/1066		Range (1.25V) DDR3U-1333		Range (1.25V) DDR3U-1600	
	Min	Nom	Max	Min	Max	Min	Max	Min	Max
Light	22	26	30	1.8	-	1.8	-	1.8	-
Moderate	16	19	22	1.8	-	1.8	-	1.8	-
Strong	12	14	16	1.8		1.8	-	1.8	-

Table 23 — RC3: CA Signals Driver Characteristics Control Word

| Input | | | | Definition | Encoding |
DBA1	DBA0	DA4	DA3		
x	x	0	0	Command/Address Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	Command/Address Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Reserved

1. DCS[n:0]# indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. QxCS[n:0] indicates all of the chip select outputs.

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 40

Table 24 — RC4: Control Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Control Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Reserved
x	x	1	1		Reserved
0	0	x	x	Control Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Reserved
1	1	x	x		Reserved

Table 25 — RC5: CK Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Clock Y1, Y1#, Y3, and Y3# Output Drivers	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	Clock Y0, Y0#, Y2, and Y2# Output Drivers	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Reserved

Exhibit 64

Case 1:Case 612053-0N294DACADAmenit13enFile47-64/15/21d 07/21/1091 Pa806464aof76D #: 680
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 41

PASS-HOLD

Table 26 — RC8 - Additional IBT Setting Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	IBT Compatibility Settings	IBT as defined in RC2
0	x	x	x	Mirror Mode	IBT Off when MIRROR is 'HIGH'[1]
1	x	x	x		IBT On when MIRROR is 'HIGH'[2]
x	0	0	1	Input Bus Termination[1]	Reserved
x	0	1	0		200 Ohm
x	0	1	1		Reserved
x	1	0	0		300 Ohm
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Off[3]

1. If MIRROR is 'HIGH' then Input Bus Termination (IBT) is turned off on all inputs, except DCSn# and DODTn inputs.
2. When DBA0 = 1, DA4 = 1, DA3 = 1, IBT on all inputs is turned off irrespective of DBA1 setting.
3. With this setting, irrespective of the logic level of the MIRROR input pin, IBT on all inputs (including DCSn# and DODTn) is turned off.

Table 27 — RC9: Power Saving Settings Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Weak Drive Mode[1] (when DCSn# = HIGH, DA3=1, and RC0 [DA4=1])	"Floating Outputs" as defined in RC0 [DA4]
x	x	x	1		Weak Drive enabled Weak Drive Impedance: 70 Ohm (min), 100 Ohm (nom), 120 Ohm (max)
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
1	0	x	x	CKE Power Down Mode	CKE power down with IBT ON, QxODT is a function of DxODT
1	1	x	x		CKE power down with IBT off, QxODT held LOW
0	x	x	x	CKE Power Down Mode Enable	Disabled
1	x	x	x		Enabled

1. When all DCS# pins are HIGH (i.e. SDRAM is in deselected state), there is no memory access to the DRAM, and the Register output can either be in a Normal Drive Mode, floated, or driven under Weak Drive Mode. A Weak Drive Mode is a mode in which CA signal output drivers (QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#) will be driven 2.5 to 3 times weaker than the Light Drive as specified in RC3, and the SDRAM VIL/VIH DC limit will be maintained. The Weak Drive Mode entry and exit timing is bounded by tDIS and tEN respectively.

The SSTE32882 register supports different power down modes. By default, the Power Down feature is disabled (RC9[DBA1]=0). The register ignores CKE Power Down mode setting when this function is dis-

Exhibit 64

abled. If the CKE Power Down mode is enabled (RC9[DBA1]=1), then power down is invoked once both DCKE0 and DCKE1 are LOW. Bit DBA0 selects how IBT and ODT behaves.

Table 28 — RC10: Encoding for RDIMM Operating Speed

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	$f \leq 800$ MTS	DDR3/DDR3L/DDR3U-800 (default)
x	0	0	1	800 MTS < $f \leq 1066$ MTS	DDR3/DDR3L/DDR3U-1066
x	0	1	0	1066 MTS < $f \leq 1333$ MTS	DDR3/DDR3L/DDR3U-1333
x	0	1	1	1333 MTS < $f \leq 1600$ MTS	DDR3/DDR3L/DDR3U-1600
x	1	0	0	Reserved	Reserved
x	1	0	1	Reserved	Reserved
x	1	1	0	Reserved	Reserved
x	1	1	1	Reserved	Reserved

Note: The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run.

RC11 will be used to inform SSTE32882 under what operating voltage V_{DD} will be used. Register can use the information to optimize their functionality and performance at DDR3U conditions.
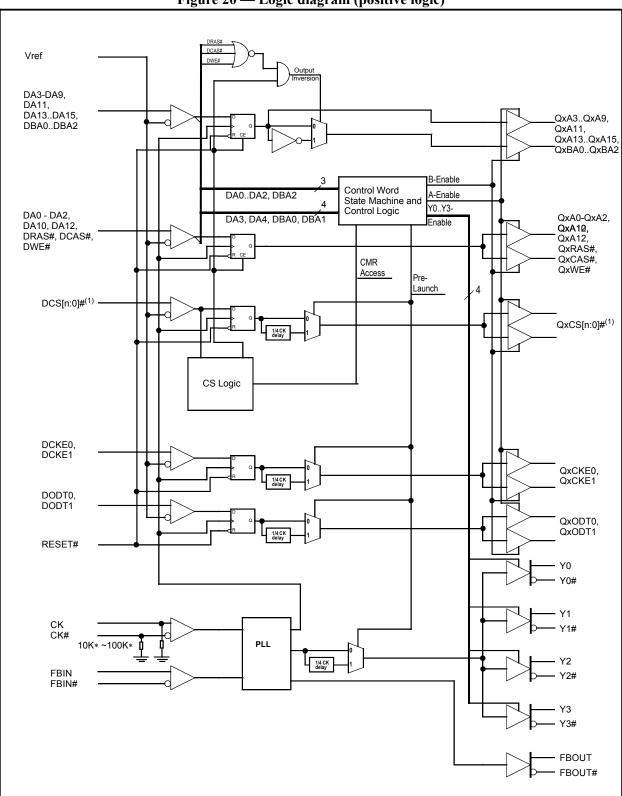
Table 29 — RC11: Operating Voltage VDD Control Word[1]

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Register V_{DD} Operating Voltage	DDR3 1.5V mode
x	x	0	1		DDR3L 1.35V mode
x	x	1	0		DDR3U 1.25V mode
x	x	1	1		Reserved
0	0	x	x		Reserved
0	1	x	x		Reserved
1	0	x	x		Reserved
1	1	x	x		Reserved

1. DDR3U 1.25V register is backward compatible and operable to DDR3 & DDR3L specification. To guarantee all timings and specifications for DDR3 & DDR3L, the register must be configured with RC11[DA4:DA3]=00b.

Exhibit 64

2.9 Logic diagram
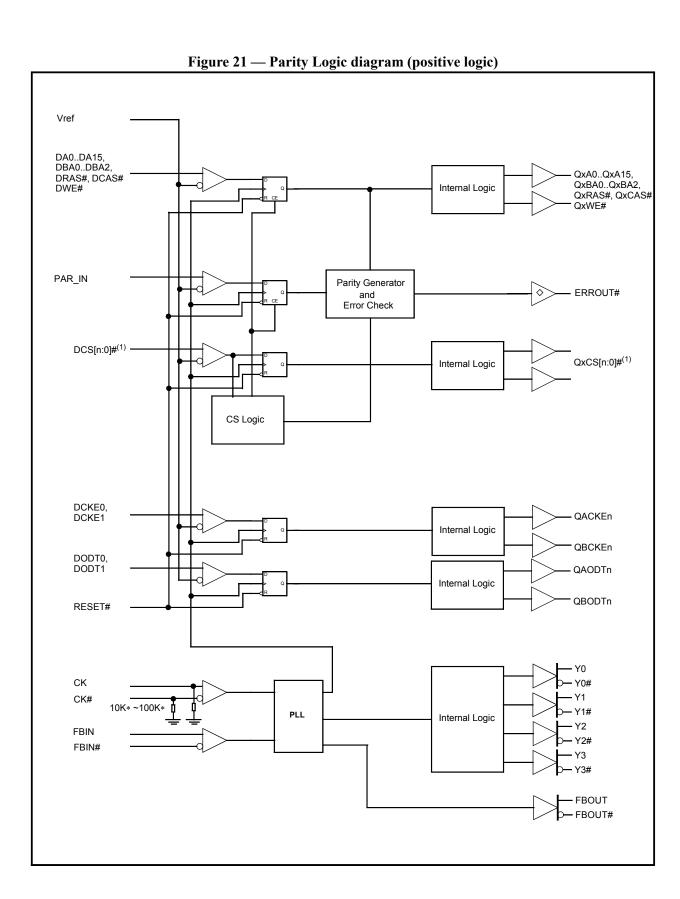
Figure 20 — Logic diagram (positive logic)

PASS-HOLD

Exhibit 64

Figure 21 — Parity Logic diagram (positive logic)

PASS-HOLD

Exhibit 64

Case 1:Case 6:05-cv-00494-DAD Document 147-60/15/21 Page 195 Page 6 of 76 ID #: 684
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 45

2.10 Absolute maximum ratings

Table 30 — Absolute maximum ratings over operating free-air temperature range [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		−0.4	+1.975	V
V_I	Receiver input voltage	See Note 2 and 3	−0.4	$V_{DD} + 0.5$	V
V_{REF}	Reference voltage		−0.4	$V_{DD} + 0.5$	V
V_O	Driver output voltage	See Note 2 and 3	−0.4	$V_{DD} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	-	-50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	-	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	Storage temperature		−65	+150	×C

NOTE 1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 1.975 V maximum.

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 46

2.11 DC and AC Specifications

The SSTE32882 parametric values are specified for the device default control word settings, unless otherwise stated. Note that the RC10 setting does not affect any of the parametric values.

Table 31 — Operating Electrical Characteristics

Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage (1.25V Operation)		1.	1.25	1.	V
V_{REF}	DC Reference voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
V_{TT}	DC Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
$V_{IH(AC)}$	AC HIGH-level input voltage (1.25V Operation, DDR3U-800/1066/1333/1600)	Data inputs[1]	V_{REF} + 135 mV	–	V_{DD} + 0.2	V
$V_{IL(AC)}$	AC LOW-level input voltage (1.5V Operation, DDR3-800/1066/1333/1600)	Data inputs[1]	–0.2	–	V_{REF} – 135 mV	V
$V_{IH(DC)}$	DC HIGH-level input voltage(1.25V Operation)	Data inputs[1]	V_{REF} + 90 mV	–	V_{DD} + 0.2	V
$V_{IL(DC)}$	DC LOW-level input voltage(1.5V Operation)	Data inputs[1]	–0.2	–	V_{REF} – 90 mV	V
$V_{IH(CMOS)}$	HIGH-level input voltage	CMOS inputs[2]	0.65 x VDD	–	V_{DD}	V
$V_{IL(CMOS)}$	LOW-level input voltage	CMOS inputs[2]	0	–	0.35 x VDD	V
$V_{IL (Static)}$	Static LOW-level input voltage[3]	CK, CK#,	-	–	0.35 x VDD	V
$V_{IX(AC)}$	Differential input crosspoint voltage range(1.25V Operation, DDR3U-800/1066/1333/1600)	CK, CK#, FBIN, FBIN#	0.5xV_{DD} - 150 mV	0.5 x V_{DD}	0.5xV_{DD} + 150 mV	V
			0.5xV_{DD} - 180 mV[4]	0.5 x V_{DD}	0.5xV_{DD} + 180 mV[5]	V
$V_{ID(AC)}$	Differential input voltage[6](1.25V Operation, DDR3-800/1066/1333)	CK, CK#	300	–	V_{DD}	mV
	Differential input voltage[6] (1.25V Operation, DDR3-1600)	CK, CK#	270	–	V_{DD}	mV
I_{OH}	HIGH-level output current[5]	All outputs except ERROUT#	-11	–	–	mA
I_{OL}	LOW-level output current[7]	All outputs except ERROUT#	11	–	—	mA
I_{OL}	LOW-level output current	ERROUT#	25	–	–	mA
V_{OD}	Differential re-driven clock swing (1.25V Operation)	Yn, Yn#	450	–	V_{DD}	mV
V_{OX}	Differential Output Crosspoint Voltage (1.25V Operation)	Yn, Yn#	0.5xV_{DD} – 90 mV	–	0.5xV_{DD} + 90 mV	V
		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	
$T_{case (max)}$	Case temperature[6]	109[9]	108[9]	106[9]	103[7]	°C

1. DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW.
2. RESET#, MIRROR
3. This spec applies only when both CK and CK# are actively driven LOW. It does not apply when CK/CK# are floating.
4. Extended range for Vix is only allowed for clock (CK and CK#) and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - CK# is larger than 3.6 V/ns
5. Default settings
6. Measurement procedure JESD51-2
7. This spec is meant to guarantee a Tj of 125C by the SSTE32882 device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a SSTE32882 device shall not be higher than 125 °C.

PASS-HOLD

Exhibit 64

2.12 DC specifications, IDD Specifications

Table 32 — DC Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	$I_{OH} = -11$ mA	V_{DD}-0.4	-	-	V
V_{OL}	Output LOW voltage	$I_{OL} = 11$ mA	-	-	0.4	V
V_{OL}	Output LOW voltage ERROUT#	$I_{OL} = 25$ mA	-	-	0.4	V
I_I	Input current	RESET#, MIRROR, $V_I = V_{DD}$ or GND	-	-	±5	∝A
I_I	Input current	QCSEN#, $V_I = V_{DD}$ or GND	-150		5	∝A
I_{ID}	Input current	Data inputs[1], $V_I = V_{DD}$ or GND	-	-	±5	∝A
I_{ID}	Input current	CK, CK#[2]; $V_I = V_{DD}$ or GND	-5		150	∝A
I_{DD}	Static standby current	RESET# = GND and CK, CK# = V_{IL}	-	-	5	mA
	Static operating current	RESET# = V_{DD}, MIRROR=V_{DD}, RC8=X111, IBT OFF, Clock inputs not switching (held static LOW), $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	15	mA
I_{DDD}	Dynamic operating current — input clock only	RESET# = V_{DD}; MIRROR=V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and CK# switching at 50% duty cycle. $I_O = 0$; $V_{DD} = V_{DD}(max)$	-	vs[3]	-	mA/MHz
	Dynamic operating current — per each data input	RESET# = V_{DD}; MIRROR=VDD, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and CK# switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. $I_O = 0$; $V_{DD} = V_{DD}(max)$	-	vs[3]	-	mA/MHz

1. DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DRAS#, DCAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW are measured while RESET# pulled LOW.
2. The CK and CK# inputs have internal pull-down resistors in the range of 10K∗ to 100K∗.
3. Vendor Specific, must be supplied by register vendor for full device description.

Table 33 — Capacitance values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input capacitance, Data inputs	see footnote[1,2]	1.5	-	2.5	pF
	Input capacitance, CK, CK#, FBIN, FBIN#	see footnote[1]	1.5	-	2.5	pF
~~C_O~~	~~Output capacitance, Re-driven and Clock Outputs~~	~~QxA0..QxA15, QxBA0..QxBA2, QxCS0/1#, QxCKE0/1, QxODT0/1, QxRAS#, QxCAS#, QxWE#, Y0, Y0#.. Y3, Y3#~~	~~1~~	~~-~~	~~2~~	~~pF~~
C_{I*}	Delta capacitance over all inputs		-	-	0.5	pF
C_{IR}	Input capacitance, RESET#, MIRROR, QCSEN#	$V_I = V_{DD}$ or GND; $V_{DD} = 1.5V$	-	-	3	pF

1. This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with VDD, VSS, AVDD, AVSS, PVDD, PVSS, V_{REF} applied and all other pins (except the pin under test) floating. Input capacitance are measured with the device default settings when MIRROR=LOW.
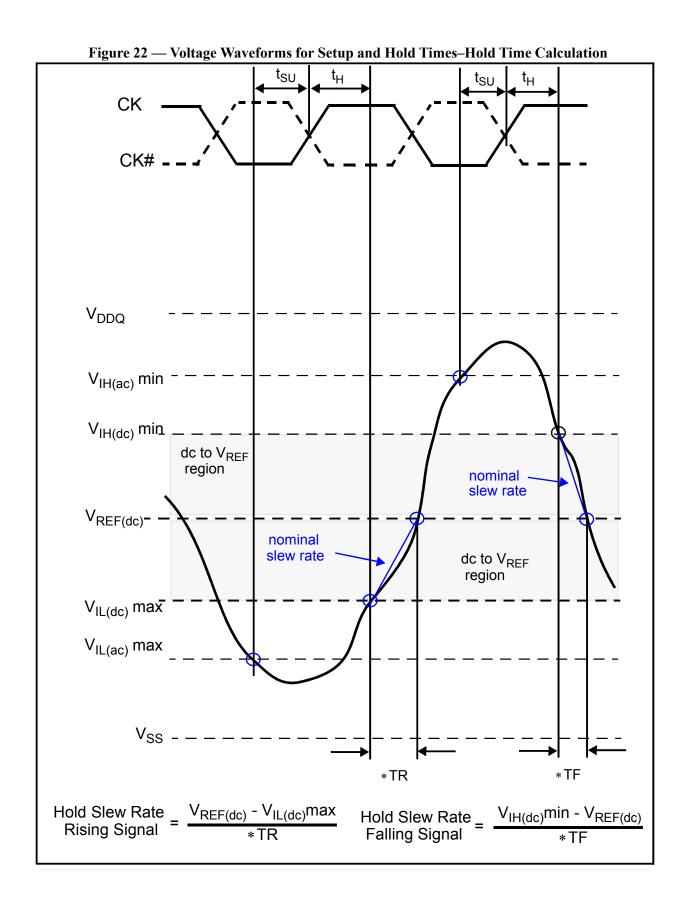2. Data inputs are DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, DCAS#, DRAS#, DWE#, PAR_IN, DCS[1:0]# when QCSEN# = HIGH, DCS[3:0]# when QCSEN# = LOW.
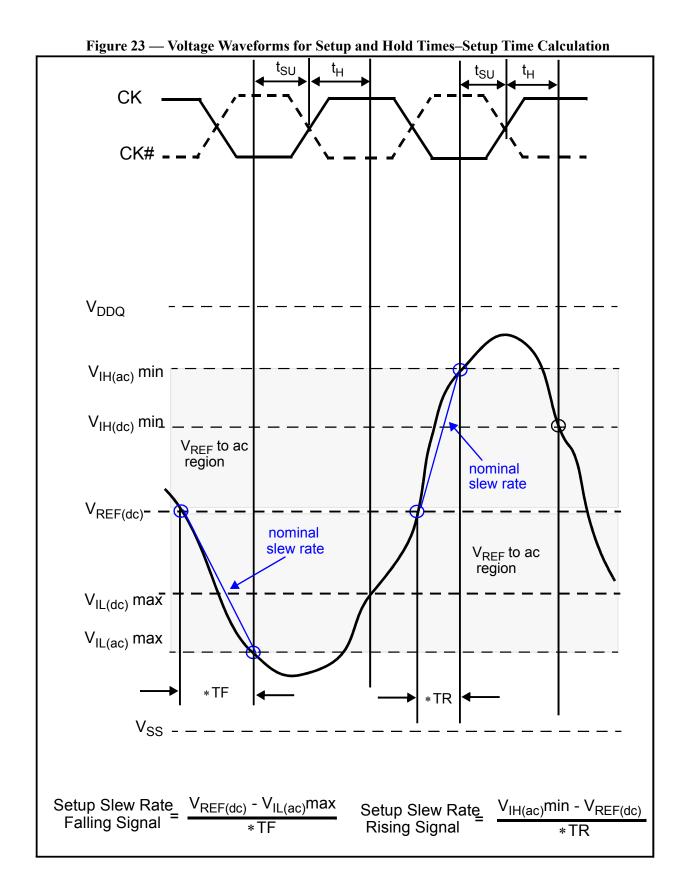
Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 48

2.13 Timing requirements

Table 34 — Timing requirements

Symbol	Parameter	Conditions	DDR3U-800/1066		DDR3U-1333/1600		Unit
			Min	Max	Min	Max	
f_{clock}	Input clock frequency	application frequency[1]			300	810	MHz
f_{TEST}	Input clock frequency	Test frequency[2]			70	300	MHz
t_{CH}/t_{CL}	Pulse duration, CK, CK# HIGH or LOW				0.4	-	t_{CK}[3]
t_{ACT}	Inputs active time[4] before RESET# is taken HIGH	DCKE0/1=LOW and DCS[n:0]#=HIGH			8	-	t_{CK}[3]
t_{MRD}	Command word to command word programming delay	Number of clock cycles between two command programming accesses			8	-	t_{CK}[3]
t_{InDIS}	Input buffers (except for CK/CK#, DCKEn, DODTn and RESET#) disable time after DCKE[1:0] is LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling; RC9[DBA1]=1 and RC9[DBA0]= 0 or 1			1	4	t_{CK}[3]
t_{QDIS}	Output buffers (except for Yn/Yn#, QxCKEn, QxODTn and FBOUT/FBOUT#) hi-z after QxCKEn is driven LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = toggling; RC9[DBA1]=1 and RC9[DBA0]=0 or 1			1.5	1.5	t_{CK}[3]
t_{CKoff}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/CK# are driven LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = Toggling			5	-	t_{CK}
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after Ck/CK# = LOW	DCKE[1:0] = LOW; RESET# = HIGH; CK/CK# = LOW			2	-	t_{CK}
$t_{Fixedoutput}$	Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state)	RC9[DBA1]=1 and RC9[DBA0]=0 or 1			1	4	t_{CK}[3]
t_{SU}	Setup time[5]	Input valid before CK/CK#			50	-	ps
t_{H}	Hold time[6]	Input to remain valid after CK/CK#			125	-	ps

1.   All specified timing parameters apply
2.   Timing parameters specified for frequency band 2 apply
3.   Clock cycle time
4.   This parameter is not necessarily production tested (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation").
5.   Setup (t_{SU}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and first crossing of $V_{IH(ac)}$min. Setup (t_{SU}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation"). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation").
6.   Hold (t_{H}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{H}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$ (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation"). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 22, "Voltage Waveforms for Setup and Hold Times–Hold Time Calculation").

Exhibit 64

Figure 22 — Voltage Waveforms for Setup and Hold Times–Hold Time Calculation

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{*TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{*TF}$$

Exhibit 64

Figure 23 — Voltage Waveforms for Setup and Hold Times–Setup Time Calculation

PASS-HOLD

$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}\text{max}}{*TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}\text{min} - V_{REF(dc)}}{*TR}$$
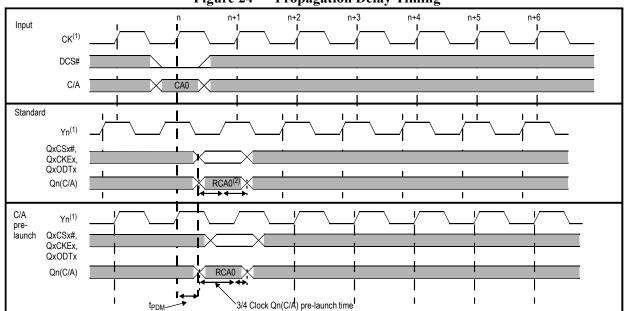
Exhibit 64

2.14 AC specifications

Table 35 — Output timing requirements (see section 3.1)[1]

Symbol	Parameter	Conditions	DDR3U-800/1066		DDR3U-1333/1600		Unit
			Min	Max	Min	Max	
t_{PDM}	Propagation delay, single-bit switching (1.25V Operation)	CK/CK# to output[2]	0.65	1.2	0.65	1.2	ns
t_{DIS}	Output disable time (1/2-Clock pre-launch)	Yn/Yn# to output float[3]	0.5 + tQSK1(min)	-	0.5 + tQSK1(min)	-	ps
	Output disable time (3/4-Clock pre-launch)		0.25 + tQSK2(min)	-	0.25 + tQSK2(min)	-	ps
t_{EN}	Output enable time (1/2-Clock pre-launch)	Output driving to Yn/Yn#	0.5 - tQSK1(max)	-	0.5 - tQSK1(max)	-	ps
	Output enable time (3/4-Clock pre-launch)		0.75 - tQSK2(max)	-	0.75 - tQSK2(max)	-	ps

1. See diagram (Figure 30, "Qn and Yn Load circuit for propagation delay and slew measurement")
2. See diagram (Figure 24, "Propagation Delay Timing")
3. See diagram (Figure 32, "Voltage waveforms address floating")

Figure 24 — Propagation Delay Timing

(1) CK# and Yn# left out for better visibility
(2) RCA0 is re-driven command address signal based on input CA0

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 52

2.15 Output buffer characteristics

Table 36 — Output edge rates over specified operating free-air temperature range

Symbol	Parameter	Conditions	DDR3U-800/1066		DDR3U-1333/1600		Unit
			Min	Max	Min	Max	
dV/dt_r	rising edge slew rate [1](1.25V Operation)		1.8	5	1.8	5	V/ns
dV/dt_f	falling edge slew rate [1](1.25V Operation)		1.8	5	1.8	5	V/ns
dV/dt_D[1]	absolute difference between dV/dt_r and dV/dt_f[1]		-	1	-	1	V/ns

1. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

2.16 Input buffer characteristics

Table 37 — Input IBT characteristics over specified operating free-air temperature range

Symbol	Parameter	Conditions	DDR3U-800/1066/1333/1600		Unit
			Min	Max	
$R_{IBT(tol)}$	Total Effective IBT Value Tolerance [1]		-10	10	%
R_{IBT*}	Total Effective IBT Value Tolerance [2]		-	5	%

1. Example for 100 ohm, Min = 90 ohm, Max = 110 ohm
2. $(1 - R_{IBT-UP}/R_{IBT-DOWN}) * 100\% <= ABS(5\%)$

Exhibit 64

Case 1:23-cv-01053-UNA Document 1-3 Filed 10/15/21 Page 68 of 76 PageID #: 692
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 53

2.17 Clock driver Characteristics

Table 38 — Clock driver Characteristics at application frequency (frequency band 1)

Symbol	Parameter	Conditions	DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{jit(cc+)}$	Cycle-to-cycle period jitter		0	40	0	40	0	40	0	30	ps
$t_{jit(cc-)}$	Cycle-to-cycle period jitter		-40	0	-40	0	-40	0	-30	0	ps
t_{STAB}	Stabilization time		-	6	-	6	-	6	-	6	us
t_{fdyn}	Dynamic phase offset		-50	50	-50	50	-50	50	-40	40	ps
t_{CKsk}	Fractional Clock Output skew[1]		-	15	-	15	-	15	-	10	ps
$t_{jit(per)}$	Yn Clock Period jitter		-40	40	-40	40	-40	40	-30	30	ps
$t_{jit(hper)}$	Half period jitter		-50	50	-50	50	-50	50	-40	40	ps
$t_{PWH/PWL}$	Yn pulse width HIGH/LOW duration[2]	t_{PW} = 1/2tCK - |t_{jit}(hper)min| to 1/2tCK + |t_{jit}(hper)max|	1.200	1.300	0.888	0.988	0.700	0.800	0.585	0.665	ns
t_{Qsk1}[3]	Qn Output to Yn clock tolerance (Standard 1/2-Clock Pre-Launch)	Output Inversion enabled	-100	200	-100	200	-100	200	-100	100	ps
		Output Inversion disabled	-100	300	-100	300	-100	300	-100	200	
t_{Qsk2}[4]	Qn Output to Yn clock tolerance (3/4 Clock Pre-Launch)	Output Inversion enabled	-100	200	-100	200	-100	200	-100	100	ps
		Output Inversion disabled	-100	300	-100	300	-100	300	-100	200	
t_{staoff}	Average delay through the register between the input clock and output clock[5].(1.5V Operation)	Standard 1/2-Clock Pre-Launch t_{staoff} = t_{PDM} + 1/2 tCK	1.90	2.25	1.59	1.94	1.40	1.75	1.28	1.63	ns
		3/4 Clock Pre-Launch t_{staoff} = t_{PDM} + 3/4 tCK	2.53	2.88	2.06	2.41	1.77	2.12	1.59	1.94	ns
	Average delay through the register between the input clock and output clock[5].(1.35V Operation)	Standard 1/2-Clock Pre-Launch t_{staoff} = t_{PDM} + 1/2 tCK	1.90	2.45	1.59	2.14	1.40	1.95	1.28	1.83	ns
		3/4 Clock Pre-Launch t_{staoff} = t_{PDM} + 3/4 tCK	2.53	3.08	2.06	2.61	1.77	2.32	1.59	2.14	ns
t_{dynoff}[6]	Maximum variation in delay between the input & output clock		-	160	-	130	-	110	-	90	ps

1. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 26, "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between Y0/Y0# and Y2/Y2#, as well as left side of the clock pairs between Y1/Y1# and Y3/Y3#. This is not a tested parameter and has to be considered as a design goal only.

2. This parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on t_{PW}.

3. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 27, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.

4. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 28, "Qn Output Skew for 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.

5. This parameter measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. t_{staoff} may vary by the amount of t_{dynoff} based on voltage and temperature drift as well as tracking error and jitter. Including this variation t_{staoff} may not exceed the limits set by $t_{staoff(min)}$ and $t_{staoff(max)}$
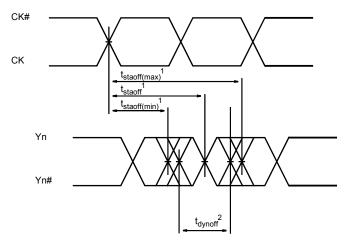
6. See Figure 25, "Definition for t_{staoff} and t_{dynoff}"

Exhibit 64

Table 39 — Clock driver Characteristics at application frequency (frequency band 1)

Symbol	Parameter	Conditions	DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
The PLL in the SSTE32882 must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:											
	SSC modulation frequency		30	33	30	33	30	33	30	33	kHz
	SSC clock input frequency deviation		0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	%
SSTE32882 PLL designs should target the values below to improve tracking between CK/CK# and Yn/Yn#:											
t_{band}	PLL Loop bandwidth (-3 dB from unity gain)		25^1	-	30^1	-	35^1	-	40^1	-	Mhz

1. Implies a -3 dB bandwidth and jitter peaking of 3 dB.

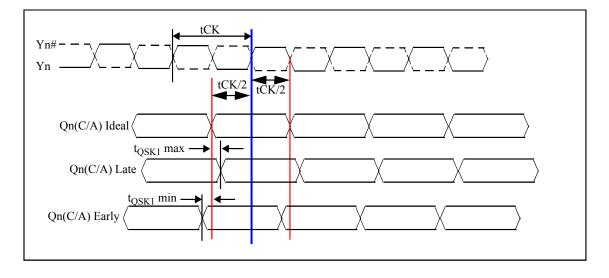**Figure 25 — Definition for t_{staoff} and t_{dynoff}**

1. t_{staoff} = propagation delay for clock signal (rising CK input clock edge to rising Yn output clock edge).

2. t_{dynoff} = maximum t_{staoff} variation over voltage and temperature.
     This includes all sources of jitter and drift (e.g.Thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

Case 1:Case 612053-0N294DoDAmPocu3lneFile47-6d/15/21d 07/21/205 Pa30f6Pagfke #: 694
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am

Page 55

Figure 26 — Clock Output (Yn) Skew

Figure 27 — Qn Output Skew for Standard 1/2-Clock Pre-Launch
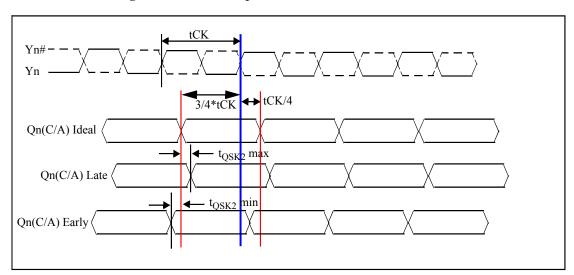

PASS-HOLD

Exhibit 64

Figure 28 — Qn Output Skew for 3/4-Clock Pre-Launch

Table 40 — Clock driver Characteristics at test frequency (frequency band 2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{jit}(cc)$	Cycle-to-cycle period jitter		0	160	ps
t_{STAB}	Stabilization time		-	15	us
t_{CKsk}	Total Clock Output Skew[1]			100	ps
	Fractional Clock Output skew[2]			vs[3]	ps
$t_{jit}(per)$	Yn Clock Period jitter		-160	160	ps
$t_{jit}(hper)$	Half period jitter		-200	200	ps
t_{Qsk1}[4]	Qn Output to clock tolerance (Standard 1/2-Clock Pre-Launch)	Output Inversion enabled	-100	vs[3]	ps
		Output Inversion disabled	-100	vs[3]	
t_{Qsk2}[5]	Output clock tolerance (3/4 Clock Pre-Launch)	Output Inversion enabled	-100	vs[3]	ps
		Output Inversion disabled	-100	vs[3]	
t_{dynoff}	Maximum re-driven dynamic clock offset[6]		-500	500	ps

1. This skew represents the absolute output clock skew and contains the pad skew and package skew.
2. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 26, "Clock Output (Yn) Skew")
3. Vendor Specific
4. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 27, "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.
5. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 28, "Qn Output Skew for 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.
6. The re-driven clock signal is ideally centered in the address/control signal eye. This parameter describes the dynamic deviation from this ideal position including jitter and dynamic phase offset.

Exhibit 64

Case 1:23-cv-01043-UNA Document 1-3 Filed 07/21/21 Page 62 of 76 Case 1:21-cv-01045-UNA Document 1-3 Filed 07/21/21 Page 207 of 306 PageID #: 696
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 57

3 Test circuits and switching waveforms

3.1 Parameter measurement information

All input pulses are supplied by generators having the following characteristics: 300MHz ∗ PRR ∗ 810MHz; Z_o = 50 ∗ ; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

Figure 29 — Voltage waveforms; input clock

.

Figure 30 — Qn and Yn Load circuit for propagation delay and slew measurement

(1) C_L is parasitic (probe and jig capacitance)

Figure 31 — Voltage waveforms; propagation delay times

V_{TT} = V_{DD}/2

V_{ICR} Cross Point Voltage

$V_{i(P-P)}$ = 500mV (1.5V Operation) or 450mV (1.35V Operation).

t_{PDM1}, t_{PDM2} the larger number of both has to be taken when performing t_{PDM} max measurement, the smaller number of both has to be taken when performing t_{PDM} min measurement

Exhibit 64

Figure 32 — Voltage waveforms address floating

1. See Figure 33, "Calculating the virtual VTT crossing point"

.Enabling and disabling the CA outputs must not violate DRAM setup and hold time requirements. Therefore a t_{DIS} transition may not occur earlier than the earliest (HL/LH) transition and a t_{EN} transition may not occur later than the latest (HL/LH) transition. Regular transitions are measured between CK/CK# and CA/V_{TT} crossings however a V_{TT} crossing is not available in the state where the outputs are Hi-Z. To allow a correct and not overly conservative measurement a virtual V_{TT} crossing point is defined below. The calculation of the virtual V_{TT} crossing point is shown in Figure 31. The voltage levels for y_{xa} and y_{xb} are measured from V_{TT} ($V_{DD}/2$) and should be selected such that the region between t1 and t2 covers a linear range and represents a typical slope of the waveform within the transition area. They have to be used signed in the formula.

PASS-HOLD

Exhibit 64

Case 1:23-cv-01055-ADA Document 36 Filed 07/21/209 Page 64 of 76 #: 698
JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 59

PASS-HOLD

Figure 33 — Calculating the virtual V_{TT} crossing point

$$t_{EN} = t_{1a} + y_{1a}(t_{1a}-t_{2a})/(y_{2a}-y_{1a}) \qquad t_{DIS} = t_{1b} + y_{1b}(t_{1b}-t_{2b})/(y_{2b}-y_{1b})$$

Figure 34 — Voltage waveforms, HIGH-to-LOW slew rate measurement

1. See Table 41

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 60

Figure 35 — Voltage waveforms, LOW-to-HIGH slew rate measurement

1. See Table 41

Table 41 — AC level for Slew Rate Measurement

	DDR3U-800/1066/1333/1600
AC Level (1.25V)	XXX mV

Exhibit 64

3.2 Error output load circuit and voltage measurement information

All input pulses are supplied by generators having the following characteristics: 300MHz $*$ PRR $*$ 810MHz; Z_o = 50 $*$; input slew rate = 1 V/ns $\pm$ 20%, unless otherwise specified.

Figure 36 — Load circuit, ERROUT# Outputs

(1) C_L includes probe and jig capacitance.

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

CA Signals =QxA0-QxAn, QxBA0-QxBAn, QxRAS#, QxCAS#, QxWE#

Control Signals = QxCSn#, QxCKEn, QxODTn

CK = Yn .. Yn#

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 62

4 Recommended Filtering for the Analog Power supply (AVDD)

Figure 37 — AVDD Filtering

Place the 2200pF capacitor close to the PLL

Use a wide trace for the PLL analog power & ground. Connect PLL & caps to AGND trace & connect trace to one GND via (farthest from PLL).

Bead: 0.8 Ohm DC max, 600 Ohms @ 100 MHz

Exhibit 64

5 Feedbackloop Topology for Registers with External Feedback

The SSTE32882 registering clock driver feedback path provides, when used by the device, compensation for drift caused by voltage and temperature effects. The flight time of the unloaded trace from FBOUT to FBIN must be 95 ± 15 ps to assure proper operation.

Figure 38, "External feedback loop" shows a topology proposal with the corresponding mechanical and electrical dimensions as per Table 42, "Feedback loop mechanical dimensions,". Both figure and table are for reference only. Actual values may vary according to application requirements. The overall loop length in this example is in the range of 15 mm which fits a typical DIMM stack-up The feedback loop doesn't affect post-register timing. It influences the phase relationship between pre- and post-register signalling. The register manufacturer guarantees the specified propagation delay if the user follows the feedback loop topology proposal in this paragraph.

.

Figure 38 — External feedback loop

Table 42 — Feedback loop mechanical dimensions

TL0		TL1	TL2	TL3	R	C
Min	Max					
12.4	12.6	2.5	0.6	1.0	equals R_{TERM} of Yn/Yn#	0 pF typ[1]

1. Pads should be present as parasitics are part of the feedback loop. If pads are not present feedback loop length must be corrected.

Exhibit 64

6 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*

JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*

JESD21-C, *Configuration for Solid State Memories.*

JESD8-11A, *Definition of wide range non-terminated logic*

Exhibit 64

7 Summary of Changes

Changes made to the document base on the December-2006 JEDEC Meeting discussions:

PASS-HOLD

Exhibit 64

JEDEC Standard No. xx-x - last edited: June 4, 2009 5:43 am
Page 66

PASS-HOLD

Exhibit 64

PASS-HOLD

Exhibit 64

PASS-HOLD

Exhibit 64

PASS-HOLD

(This page is intentionally left blank)

Exhibit 64

Exhibit 64

EXHIBIT P

JEDEC

Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
TEL: (703) 907-7560
FAX: (703) 907-7583
http://www.jedec.org

COMMITTEE LETTER BALLOT

COMMITTEE: JC-40.4

Committee Item Number: 142.35

Subject: LRDIMM DDR3 Memory Initialization Chapter Proposal

Background: At September '09 JEDEC meeting in San Jose, "motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the items listed on pages 3 and 4 of the presentation that have item numbers, have been shown in the committee and for which the TG has reached a consensus".

The motion passed by acclamation.

This ballot proposal is to specify LRDIMM DDR3 Memory Initialization, and has been approved by DDR3 MB TG on 11/09/2009.

Keywords: DDR3, MB, Memory Buffer, LRDIMM, Initialization

P R O P O S E D

(This page is intentionally left blank)

Exhibit 65

6 Initialization

6.1 Initialization Overview

The sequence of steps below is an overview of the power-up initialization of the Memory Buffer. Figure 1 shows a graphical representation of the same steps. Detailed requirements for each step are provided in the following sections. Note that the sequence below does not distinguish between host HW and host SW (i.e. BIOS).

1. Power-Up (Same requirements as 882)
    a. Ramp of voltage rails
    b. Generation of stable clock
    c. De-assertion of RESET#
2. Determination of DIMM configuration via SPD read out
3. CA Clock to CMD Training[1]
    a. Sets the optimal phase of the clock to CA and Ctrl signals.
4. Memory Buffer Initialization
    a. Host initializes buffer control words
5. DRAM Initialization
    a. Host initializes DRAM MRS registers
6. DRAM ZQ Calibration
    a. Host issues ZQCAL command to DRAM
7. Memory Buffer to DRAM Interface Training
    a. Done by the buffer, triggered by host RCW write
    b. Write Leveling
    c. Read Enable training
    d. Read/Write DQ/DQS training[2]

Host can wait for a per-physical rank time-out of tCAL=10ms or periodically poll the buffer via SMBus CSR read or wait for ERROUT#.

8. Host to Memory Buffer Interface Training[3]
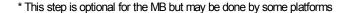   a. Done by host
9. Normal Operation

PROPOSED

---

1. This step is optional for the MB but may be done by some platforms. No special support by the MB is required.
2. This step is optional for the MB but may be required for stable DIMM operation.
3. This step is optional for the MB but may be done by some platforms.

Exhibit 65

Figure 1 — Initialization Overview

PROPOSED

```
┌─────────────────────────────────────────────┐
│              Power-Up                         │
│                                               │
│              SPD Readout                      │
│                                               │
│     Host Interface CA Clk-to-CMD Training*    │
│                                               │
│              MB Initialization                │
│                                               │
│              DRAM Initialization              │
│                                               │
│              DRAM ZQ Calibration              │
│                                               │
│          MB-DRAM Interface Training           │
│                                               │
│              Host-MB Training*                │
│                                               │
│              Normal Operation                 │
└─────────────────────────────────────────────┘
```

* This step is optional for the MB but may be done by some platforms

6.2 Power-on Initialization

The Memory Buffer can be powered-on at 1.5V or 1.35V. After the voltage ramp, stable power is provided for a minimum of 200 uS with RESET# asserted. When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. The MB output pin QRST# follows the MB input pin RESET#. Therefore the reference voltage (V_{REF}) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE[3:0] and QBCKE[3:0] must drive LOW during reset. All other outputs must float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[1:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE[2:0] as well as DCKE3/DODT[1] must be pulled LOW.

Case 1:23-cv-01043-UNA Document 1-3 Filed 07/21/21 Page 12 of 12 Page ID #: 716
Case 1:21-cv-00194-DA Document 1-3 Filed 06/15/21 Page 227 of 306 Page 12

Item 142.35

6.2.1 Clock Stabilizaion Time t_{STAB}

During PLL stabilization time t_{STAB} the memory buffer is not fully operational. In order to avoid invalid comands being sent to the DRAMs some rules apply to the inputs of the buffer:

⌘ All DCS signals need to be kept high. No DRAM command or control word write[1] may take place.

⌘ All DCKE signals don't change their state.

⌘ DODT[0] or DODT[1:0] signals (depending on F0RC6 setting) are kept at a stable valid logic level.

These rules apply to any instance where stabilization time t_{STAB} is required:

⌘ Exit from Reset

⌘ Exit from clock stop power down

⌘ Changing clocking related registers (F0RC2, F0RC10, F0RC11, F1RC8, F1RC11-F1RC15)[2]

⌘ Changing input clock frequency during boot or run time

Since the buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the PLL stabilization time (t_{STAB}) the device must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be held at a valid logic level once the input clock is present.
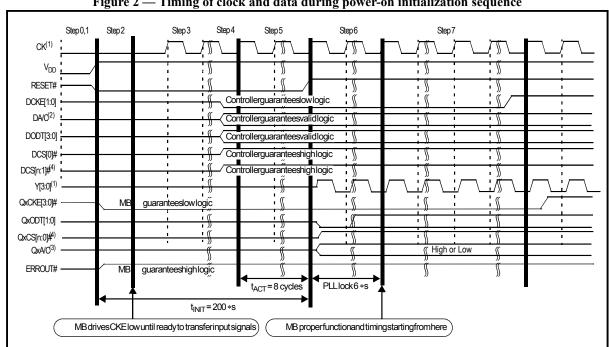
Figure 2 — Timing of clock and data during power-on initialization sequence

---

1. No control word writes are allowed during t_{STAB} after reset/frequency change/clock stop. Control word writes are allowed during t_{STAB} after clocking related register write.

2. These requirements mean that we have to wait two t_{STAB} times during every initialization, one after RESET# de-assertion and one after all the clocking related control words have been written.

Exhibit 65

PROPOSED

(1) CK# and Y[3:0]# left out for better visibility

(2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]# are not included in this range

(3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]# are not included in this range

(4) n = JEDEC standard DIMMs, n = 7 for non-JEDEC applications

(5) n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs

From a device perspective, the initialization sequence must be as shown in Table 1

Table 1 — MB Device Initialization Sequence[a]

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:0][b]	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK CK#	QCS# [n:0][c]	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUT#	Y[3:0] Y#[3:0]
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z
1	0-->VDD	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2[d]	VDD 1.5V-->1.35V 1.35V-->1.5V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L[e]	Z	H[4]	Z
3	VDD	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z
4	VDD	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z
5	VDD	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	VDD	H	stable voltage	H	X	L	X	X	running	H	L[f]	L	X	H	running
7[g]	VDD	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).					

a. X = Logic LOW or logic HIGH. Z = floating.

b. n = 3 for JEDEC standard DIMM, n = 7 for non-JEDEC application

c. n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

d. The system may power up using either 1.5V or 1.35V. The BIOS reads the SPD and adjusts the voltage if needed from 1.35V to 1.5V or from 1.5V to 1.35V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET# asserted.

e. QxCKE[3:0] and ERRROUT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5V or 1.35V (nominal).

f. This indicates the state of QxODT[1:0] after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge).

g. Step 7 is a typical usage example and is not a MB requirement.

To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3 LRDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two.

As part of the initialization all control words are reset to their default state which is "0", except when explicitly defined otherwise. After initialization, the host only needs to write to those control registers whose contents need to be changed.

6.3 Initialization with Stable Power (Soft Reset)

The timing diagram in Figure 3 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# will be asserted for minimum 100ns. This RESET# timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3 Specification.

PROPOSED

Item 142.35

Figure 3 — Timing of clock and data during initialization sequence with stable power

(1) CK# and Y[3:0]# left out for better visibility

(2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]# are not included in this range

(3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]# are not included in this range

(4) n = JEDEC standard DIMMs, n = 7 for non-JEDEC applications

(5) n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

Table 2 — MB Device Initialization Sequence[a] when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller							Outputs: Signals provided by the device					
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:0][b]	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK CK#	QCS# [n:0][c]	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUT#	Y[3:0] Y#[3:0]
0	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
1	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
2	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L[d]	Z	H[4]	Z
3	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z
4	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[e]	L	X	H	running
7	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).					

a. X = Logic LOW or logic HIGH. Z = floating.

b. n = 3 for JEDEC standard DIMM, n = 7 for non-JEDEC application

c. n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

Exhibit 65

d. QxCKE[3:0] and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and V_{DD} is nominal

e. This indicates the state of QxODT[1:0] after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge)

6.4 Host RCW to Configure MB

After the MB is ready to receive commands and addresses without error, the host needs to configure the MB with register control word writes and/or SMBUS writes (step 4). At reset all RCWs had been reset to their default state (which is '0' except when explicitly noted otherwise). Therefore the host only needs to write those control words whose contents need to be changed.

6.5 Host MRS to Configure DRAM

The host sends MRS commands to the DRAM mode registers to configure proper DRAM operation for all ranks behind the MB. The host can utilize either the MB broadcast mode to send MRS commands to all physical ranks associated with a logical rank or the MB physical rank mode to target MRS commands to specific physical ranks by programming the corresponding mode to the F0RC14 DRAM MRS Control bits.

6.6 Host MRS to DRAM ZQ Calibration

The host sends ZQCL (ZQ Calibration Long) commands to all ranks behind the MB. The MB broadcasts ZQ calibration commands (both ZQCL and ZQCS) to all physical ranks associated with a logical rank. The host may issue ZQ calibration commands sequentially to each logical rank (i.e. wait for tZQinit, tZQoper or tZQCS after each ZQ calibration command before issuing the next one) or it may overlap the ZQ calibration commands to all ranks.

The MB may or may not perform any calibration for its own I/O circuits on receipt of ZQCL or ZQCS calibration commands.

6.7 MB-DRAM Training

After all the DRAMs are fully operational, the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12. Once enabled, the MB assumes autonomous control of the Command/ Address, Control and Data/Strobe signals to the DRAMs, without any further assistance from the host.

The MB performs 'Write Leveling' to the DRAMs to ensure successful writes, and 'Read Enable Training' to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training.

No DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low. The MB responds to SMBus CSR read accesses whether or not DRAM interface training is active. To determine DRAM interface training completion the host may either wait for a time 'tCAL * number of physical ranks' (which is the maximum amount of time that the MB-DRAM Interface training is allowed to take) or it may periodically poll the content of the MB CSR 'Training Completion' (see 'Configuration Registers' chapter) over the SMBus.

In addition, training completion can be signaled by the assertion of ERROUT#. This is not the power-up default but can be enabled by setting the DBA1 bit in the F3RC14 Training Completion Control Word.

6.8 Host-MB Training

Now the host can train the MB host interface. The host sets the 'Connector DQ interface write leveling'

Item 142.35

bits in F0RC12 (=0bx001) in order to perform host interface write leveling. Optionally a MB may support RDIMM backward compatible host interface write leveling by intercepting 'Write leveling enable' (MR1 A7) and 'Qoff' (MR1 A12) commands to the DRAMs. The MB asynchronously feeds back CK/CK#, sampled with the rising edge of DQS/DQS#, through the DQ bus (in the same way as a DDR3 DRAM does). Since write leveling requests from the host terminate at the MB, multiple write leveling requests to the MB (i.e. one per rank) will give the same result and are optional. It is sufficient to perform host interface write leveling only once regardless of how many logical or physical ranks are supported by the MB.

MB DRAM interface training must be completed before any MB host interface read training to reflect the correct read round trip delay to and from an LRDIMM. This delay consists of

(1) Host to MB delay for command

(2) Command delay through the MB[1]

(3) MB command to DRAM delay

(4) DRAM latency

(5) DRAM data/strobe return time to MB

(6) Data/strobe delay through the MB

(7) MB to host delay for data/strobe

MB DRAM interface training must be completed before any MB host interface read or write training to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes. The host performs normal writes to DRAM for write DQ/DQS margining, with failure occurring through incorrect strobing of write data through the MB. The host performs read DQ/DQS margining by using normal reads from DRAM or by using the DRAM multi purpose register (MPR) with failure occurring through invalid DQ/DQS alignment at the host I/O pins. No special support by the MB is required for host interface read training.

PROPOSED

1.Note that the data/strobe delay through the MB during writes can be different than the command delay through the MB.

Name

High Quality Print.joboptions

Exhibit 65

Exhibit 65

EXHIBIT Q

JEDEC

Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
TEL: (703) 907-7560
FAX: (703) 907-7583
http://www.jedec.org

COMMITTEE LETTER BALLOT

Committee: 45.4

Committee Item Number: 2192.44

Subject: DDR3 LRDIMM Design Specification Body

Background: At the September 2009 Committee meeting the DDR3 LRDIMM TG was given authorization for 1 or more ballots on the LRDIMM Design Specification body and Appendices.

The following LRDIMM Design Specification has Change bars and Highlighted text however the **entire specification is being balloted.** The change bars and Highlighted areas are difference from the RDIMM specification.

Keywords: LRDIMM, DIMM, DDR3, MB, Memory Buffer, DRAM, SDRAM, Design, Specification

Exhibit 66

PC3 Load Reduced DIMM (LRDIMM)

Design Specification

Revision 0.16

November 4, 2009

The following draft contains general sections for DDR3 LRDIMMs.

Proposed

Contents

Proposed

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
Contents

Exhibit 66

Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 72 bit-wide, Load Reduced Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM DIMMs).These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and work-stations.

PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 refers to the JEDEC standard DIMM naming convention in which PC3-6400/PC3-8500/PC3-10600/PC-12800PC3-14900/PC3-17000 indicates a 240-pin DIMM running at 400/533/666/800/933/1066 MHz clock speed and offering 6400/8500/10600/12800/14900/17000 MB/s bandwidth.

Reference design examples are included which provide an initial basis for Load Reduced DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and ther-mal requirements. All load reduced DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

The LRDIMM differs from RDIMMs in that the SDRAMs do not connect directly to the edge connector with the exception of VDD andd VSS (ground). The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load. The maximum number of SDRAM die is 144. The LRDIMM is intended to function in all RDIMM plat-forms with appropriate BIOS changes. Systems designed to function with LRDIMMs will be better able to take advantage of LRDIMM features.

While four chip selects are possible at the edge connector the MB provides a "address multiplication" feature. The MB uses one or two of the address lines not directly useable by the SDRAM to generate additional chips selects to the SDRAM. This feature is completely configureable in the MB. There are 2 additional address lines (A16 and A17) defined that will typically only be used with the address multiplication feature. With address multiplication refresh and mode register access become more difficult. This is because the system sees the LRDIMM as fewer logical ranks that the true physical ranks. Rank based commands like refresh and mode register access must accommodate this in some fashion. The MB provides several methods. See the MB Design Specification for more information on the MB features and programming.

The LRDIMM has the option of using ODT0 only or both ODT0 and ODT1.

The VREF_DQ and VREF_CA pins on the edge connector provide the reference for the MB. The MB has additional VREF generators that may be used for the SDRAM reference and as the reference for the MB interfaces.

LRDIMMs can use an address mirroring feature. This is exactly as defined in the UDIMM Design Specifica-tion with the exception that all odd ranks are mirrored when this feature is used. There is an SPD bit that pro-vides the information to the system on whether the specific LRDIMM requires the use of address mrroring. Since the wiring on the LRDIMM is different to support this feature it must be used when the LRDIMM is wired to use address mirroring. As defined the controller must have the capability to do address mirroring.

The LRDIMMs are defined to require an integrated thermal sensor with the SPD. Additionally the MB is defined to have an internal thermal sensor.

Proposed

DDR3 SDRAM LRDIMM Design Specification
 Product Description   JEDEC internal use only

Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions : height (nom.) x width(nom.) x thickness(max.) / MO-number, Variation	30.35 mm x 133.35 mm x 4.00 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 6.75 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 7.55 mm / MO-269, Variation TBD 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation DB 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation EB 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation FB
Pin count	240
SDRAMs supported	1 Gb, 2 Gb, 4 Gb
Capacity	4 GB, 8 GB, 16 GB, 32 GB, 64 GB
Serial PD	Consistent with JC 45
Voltage options	1.35 and 1.5 volt (V_{DD}), 3.3 volt (V_{DDSPD})
Interface	1.35 and 1.5 volt signal switching based on reference voltage at VDD/2. See DRAM specification for more detail.

Environmental Parameters

DDR3 SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	°C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

Proposed

Exhibit 66

Pinout and Description

Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0_t	Clock Input, positive line	1	Par_In	Parity bit for the Address and Control bus	1
CK0_c	Clock Input, negative line	1	ErrOut_n	Parity error found on the Address and Control bus	1
CK1_t	Clock Input, positive line	1	ODT[0]	On Die Termination Input	1
CK1_c	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	CB[7:0]	Data check bits Input/Output	8
CKE[3:2], ODT[1], TEST	Clock Enables On Die Termination Memory bus tool (Not Connected and Not Useable on DIMMs)	2	DQS[8:0]_t	Data strobes	9
RAS_n	Row Address Strobe	1	DQS[8:0]_c	Data strobes, negative line	9
CAS_n	Column Address Strobe	1	DM[8:0]/ DQS[17:9]_t, TDQS[17:9]_t	Data Masks / Data strobes, Termination data strobes	9
WE_n	Write Enable	1	DQS[17:9]_c TDQS[17:9]_c	Data strobes, negative line, Termination data strobes	9
S[1:0]_n	Chip Selects	2	EVENT_n	Reserved for optional hardware temperature sensing	1
S[3:2]_n, A17, A16	Chip Selects Address Inputs	2	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
A[9:0],A11, A[15:13]	Address Inputs	14	RESET_n	Register and SDRAM control pin	1
A10/AP	Address Input/Autoprecharge	1	V_{DD}	Power Supply	22
A12/BC_n	Address Input/Burst chop	1	V_{SS}	Ground	59
BA[2:0]	SDRAM Bank Addresses	3	V_{REFDQ}	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{REFCA}	Reference Voltage for CA	1
SDA	SPD Data Input/Output	1	V_{TT}	Termination Voltage	4
SA[2:0]	SPD Address Inputs	3	V_{DDSPD}	SPD Power	1

Proposed

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
Pinout and Description
JEDEC internal use only

Load Reduced DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0_t	IN	Positive Line	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.
CK0_c	IN	Negative Line	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CK1_t	IN	Positive Line	Terminated but not used on RDIMMs.
CK1_c	IN	Negative Line	Terminated but not used on RDIMMs.
CKE[3:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[3:0]_n	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2]_n operate similarly to S[1:0]_n for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM.
V$_{REFDQ}$	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V$_{REFCA}$	Supply		Reference voltage for A0-A17, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, S2_n, S3_n, CKE0, CKE1, CKE2, CKE3, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[17:13, 12/BC_n,11, 10/AP,[9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for ''BL on the fly'' during CAS_n command. The address inputs also provide the op-code during Mode Register Set commands.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V$_{DD}$, V$_{SS}$	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V$_{TT}$	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[17:0]_t	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS[17:0]_c	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.

Exhibit 66

JEDEC internal use only

Load Reduced DIMM Input/Output Functional Description (Continued)

Symbol	Type	Polarity	Function
TDQS[17:9]_t TDQS[17:9]_c	OUT		TDQS_t/TDQS_c is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1,DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11=0 in MR1, DM/TDQS_t will provide the data mask function and TDQS_c is not used. X4/X16 DRAMs must disable the TDQS function via mode register A11=0 in MR1
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} on the system planar to act as a pullup.
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part. No pull-up resister is provided on DIMM.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN	Active Low	The RESET_n pin is connected to the RESET_n pin on the register and to the RESET_n pin on the DRAM.
Par_In	IN		Parity bit for the Address and Command bus. ("1 ": Odd, "0 ": Even)
ErrOut_n	OUT (open drain)		Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V_{DD} on the system planar to act as a pull up.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

Proposed

Exhibit 66

DDR3 240-pin LRDIMM, RDIMM and UDIMM Pinout

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{REFDQ}	121	V_{SS}	31	DQ25	151	V_{SS}	61	A2	181	A1	91	DQ41	211	V_{SS}
2	V_{SS}	122	DQ4	32	V_{SS}	152	DM3, DQS12_t, TDQS12_t	62	V_{DD}	182	V_{DD}	92	V_{SS}	212	DM5, DQS14_t, TDQS14_t
3	DQ0	123	DQ5	33	DQS3_c	153	NC,DQS12_c, TDQS12_c	63	NC, CK1_t	183	V_{DD}	93	DQS5_c	213	NC, DQS14_c, TDQS14_c
4	DQ1	124	V_{SS}	34	DQS3_t	154	V_{SS}	64	NC, CK1_c	184	CK0_t	94	DQS5_t	214	V_{SS}
5	V_{SS}	125	DM0,DQS9_t, TDQS9_t	35	V_{SS}	155	DQ30	65	V_{DD}	185	CK0_c	95	V_{SS}	215	DQ46
6	DQS0_c	126	NC,DQS9_c, TDQS9_c	36	DQ26	156	DQ31	66	V_{DD}	186	V_{DD}	96	DQ42	216	DQ47
7	DQS0_t	127	V_{SS}	37	DQ27	157	V_{SS}	67	V_{REFCA}	187	EVENT_n, NC	97	DQ43	217	V_{SS}
8	V_{SS}	128	DQ6	38	V_{SS}	158	CB4,NC	68	Par_In, NC	188	A0	98	V_{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	69	V_{DD}	189	V_{DD}	99	DQ48	219	DQ53
10	DQ3	130	V_{SS}	40	CB1,NC	160	V_{SS}	70	A10 / AP	190	BA1	100	DQ49	220	V_{SS}
11	V_{SS}	131	DQ12	41	V_{SS}	161	NC, DM8, DQS17_t, TDQS17_t,	71	BA0	191	V_{DD}	101	V_{SS}	221	DM6, DQS15_t, TDQS15_t
12	DQ8	132	DQ13	42	DQS8_c	162	NC,DQS17_c, TDQS17_c	72	V_{DD}	192	RAS_n	102	DQS6_c	222	NC, DQS15_c, TDQS15_c
13	DQ9	133	V_{SS}	43	DQS8_t	163	V_{SS}	73	WE_n	193	S0_n	103	DQS6_t	223	V_{SS}
14	V_{SS}	134	DM1, DQS10_t, TDQS10_t	44	V_{SS}	164	CB6,NC	74	CAS_n	194	V_{DD}	104	V_{SS}	224	DQ54
15	DQS1_c	135	NC, DQS10_c, TDQS10_c	45	CB2,NC	165	CB7,NC	75	V_{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1_t	136	V_{SS}	46	CB3,NC	166	V_{SS}	76	S1_n, NC	196	A13	106	DQ51	226	V_{SS}
17	V_{SS}	137	DQ14	47	V_{SS}	167	NC(TEST), CKE2	77	ODT1, CKE3, NC	197	V_{DD}	107	V_{SS}	227	DQ60
18	DQ10	138	DQ15	48	VTT, NC	168	RESET_n	78	V_{DD}	198	S3_n, A17, NC	108	DQ56	228	DQ61
19	DQ11	139	V_{SS}		KEY			79	S2_n, A16, NC	199	V_{SS}	109	DQ57	229	V_{SS}
20	V_{SS}	140	DQ20	49	VTT, NC	169	CKE1, NC	80	V_{SS}	200	DQ36	110	V_{SS}	230	DM7, DQS16_t, TDQS16_t
21	DQ16	141	DQ21	50	CKE0	170	V_{DD}	81	DQ32	201	DQ37	111	DQS7_c	231	NC, DQS16_c, TDQS16_c
22	DQ17	142	V_{SS}	51	V_{DD}	171	A15	82	DQ33	202	V_{SS}	112	DQS7_t	232	V_{SS}
23	V_{SS}	143	DM2, DQS11_t, TDQS11_t	52	BA2	172	A14	83	V_{SS}	203	DM4, DQS13_t, TDQS13_t	113	V_{SS}	233	DQ62
24	DQS2_c	144	NC, DQS11_c TDQS11_c,	53	ErrOut_n NC	173	V_{DD}	84	DQS4_c	204	NC, DQS13_c, TDQS13_c	114	DQ58	234	DQ63
25	DQS2_t	145	V_{SS}	54	V_{DD}	174	A12 / BC_n	85	DQS4_t	205	V_{SS}	115	DQ59	235	V_{SS}
26	V_{SS}	146	DQ22	55	A11	175	A9	86	V_{SS}	206	DQ38	116	V_{SS}	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	V_{DD}	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V_{SS}	57	V_{DD}	177	A8	88	DQ35	208	V_{SS}	118	SCL	238	SDA
29	V_{SS}	149	DQ28	58	A5	178	A6	89	V_{SS}	209	DQ44	119	SA2	239	V_{SS}
30	DQ24	150	DQ29	59	A4	179	VDD	90	DQ40	210	DQ45	120	V_{TT}	240	V_{TT}
				60	V_{DD}	180	A3								

Proposed

See Notes on following page for differences of RDIMMs and UDIMMs and LRDIMMs

Exhibit 66

Pinout Comparison Between UDIMM Type and LRDIMM Type

Pin #	UDIMM		LRDIMM	
	Signal	**Notes**	**Signal**	**Notes**
48, 49	NC	Not used on UDIMMs	VTT	Termination Voltage for Address/Command/Control/Clock nets.
120, 240	VTT	Termination Voltage for Address/Command/Control/Clock nets.	VTT	Termination Voltage for Address/Command/Control/Clock nets.
53	NC	Not used on UDIMMs	ERROut_n	Parity error output of Memory Buffer
63	CK1_t	Used for 2 rank UDIMMs, not used on single-rank UDIMMs, but terminated	CK1_t	Terminated but not used
64	CK1_c		CK1_c	
68	NC	Not used on UDIMMs	Par_In	Parity input to Memory Buffer (MB). This siignal is required for MB functionality.
76	S1_n	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	S1_n	Chip select for the second logical rank. Required for programming the Memory Buffer. SMBus can be used for programming the MB.
77	ODT1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	ODT1, CKE3	Provides 4th CKE signal. Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs. Connected to MB.
79	NC	Not used on UDIMMs	S2_n, A16	May be used as third chip select or address A16. Use is system dependent. MB can be programmed to use it as chip select 2 or address A16.
167	NC	TEST input used only on bus analysis probes	CKE2	Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs.
169	CKE1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	CKE1	2nd CKE.
171	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs. However, these signals are terminated on UDIMMs. A15 not routed on some RCs	A15	Always used on LRDIMMs
172	A14		A14	
196	A13		A13	
198	NC	Not used on UDIMMs	S3_n, A17	May be used as either a 4th chip select or address A17. Use is system dependent. MB can be programmed to use it as chip select 3 or address A17.
39, 40, 45, 46, 158, 159, 164, 165	NC, CBn	Used on x72 UDIMMs, (n = 0...7); not used on x64 UDIMMs	CBn	ECC byte. Always used on LRDIMM.
125, 134, 143, 152, 161, 203, 212, 221, 230	DMn	Connected to DM on x8 DRAMs, UDM or LDM on x16 DRAMs on UDIMMs; (n = 0...8)	DQS [9:17]_t	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
126, 135, 144, 153, 162, 204, 213, 222, 231	NC	Not used on UDIMMs	DQS [9:17]_c	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
187	EVENT_n NC	Connected to the thermal sensing component on ECC DIMMs. No connection on non-ECC DIMMs.	EVENT_n	Connected to the thermal sensing component and MB.

NC = no internal connection

Proposed

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
 Pinout and Description   JEDEC internal use only

Pinout Comparison Between RDIMM Type and LRDIMM Type

Pin #	RDIMM		LRDIMM	
	Signal	Notes	Signal	Notes
77	ODT1, NC	ODT1 is connected to the register on dual- and quad- rank RDIMMs; NC on single-rank RDIMMs, CKE3 is not available for RDIMMs	ODT1, NC, CKE3	ODT1, CKE3 is connected to the Memory Buffer. It has no defined functionality in normal use but is available for custom applications.
79	S2_n, NC	S2_n is connected to the register on quad-rank RDIMMs, not connected on single or dual rank RDIMMs. A16 is not available for RDIMMs	S2_n, NC, A16	S2_n, A16 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
167	NC	TEST input used only on bus analysis probes. CKE2 is not avilable for RDIMMs	NC, CKE2	TEST input used only on bus analysis probes. The CKE2 function is only available on custom modules.
198	S3_n, NC	Connected to the register on quad-rank RDIMMs, not connected on single-or-dual-rank RDIMMs	S3_n, NC, A17	S3_n, A17 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
NC = no internal connection				

Proposed

Exhibit 66

Component Details

Supported SDRAM Components Maximum size for 1Gb to 4Gb; DDR3 SDRAM
This table is for reference only. Please see appropriate raw card appendix for more information.

Raw Card	Supported DRAM Outline (Width x Length) max.	Configuration	SDRAM Placement	Package Type	Module Height (mm)	MO-207 variation	# of SDRAM balls supported
A	11.0 mm x 12.0 mm	2 rank x4	2 row vertical	Planar	30.35	DW-z	82
B	11.0 mm x 12.0 mm	4 rank x8	2 row vertical	Planar	30.35	DW-z	82
C	11.0 mm x 11.6 mm	4 rank x4	2 row vertical	DDP	30.35	DW-z	82
D	11.0 mm x 12.0 mm	8 rank x8	2 row vertical	DDP	30.35	DW-z	82
E	11.0 mm x 12.0 mm	8 rank x4	2 row vertical	QDP	30.35	DW-z	82
F	11.0 mm x 12.0 mm	2 rank x4	1 row vertical	DDP	18.75	DW-z	82
G	11.0 mm x 12.0 mm	4 rank x8	1 row vertical	DDP	18.75	DW-z	82
H	11.0 mm x 12.0 mm	4 rank x4	1 row vertical	QDP	18.75	DW-z	82
J	11.0 mm x 12.0 mm	8 rank x8	1 row vertical	QDP	18.75	DW-z	82
K	10.0 mm x 13.0 mm 11.0 mm x 12.0 mm	4 rank x4	2 row flower	DDP	30.35	DW-z	82

Note: 1. DDP refers to a 2 die stack. QDP refers to a 4 die stack.

Proposed

Exhibit 66

Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

(MO-207 Variation DT-z/DW-z, FBGA 0.8mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V_{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V_{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z

Populated ball
Ball not populated

MO-207 Variation DW-z
with support balls

Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).
Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note: 3. NC balls may be mated with any solder pad on PCB.
Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

Exhibit 66

Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

(MO-207 Variation DT-z/DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V_{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS#	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V_{REFCA}	VSS		J
R		VDD	A3	A0	A12/ BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
	1	2	3	7	8	9			

MO-207 Variation DT-z

Populated ball
Ball not populated

MO-207 Variation DW-z
with support balls

Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 21).
Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note: 3. NC balls may be mated with any solder pad on PCB.
Note: 4. "NU" means that the ball is present and may or may not be electrically connected a an active signal in the SDRAM package.
Note: 5. NU balls may only be mated with NC solder pads on PCB.
Note: 6. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

Exhibit 66

Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)
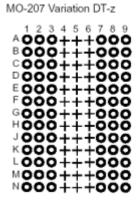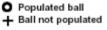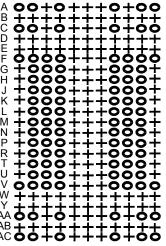
x4 Ballout of DDR3 SDRAMs for DDP Stacked DIMM (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V_{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V_{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z

○ Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls

Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 22).
Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note: 3. NC balls may be mated with any solder pad on PCB.
Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

Exhibit 66

Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs for Stacked DDP DIMM (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V_{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V_{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 22).
Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note: 3. NC balls may be mated with any solder pad on PCB.
Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

MO-207 Variation DT-z

O Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls

Proposed

Exhibit 66
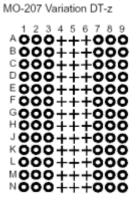
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC			NC	NC		NC	NC	
B									
C	NC	NC			NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V_{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V_{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC			NC	NC		NC	NC	
AB									
AC	NC	NC			NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z

○ Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls

Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).
Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note: 3. NC balls may be mated with any solder pad on PCB.
Note: 4.This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

Exhibit 66
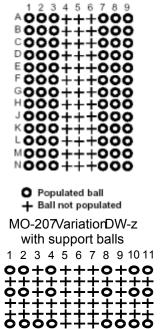
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V_{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V_{REFCA}	VSS		J
R		CS2_n	A3	A0	A12/BC_n	BA1	ZQ2		K
T		CS3_n	A5	A2	A1	A4	ZQ3		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z

O Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls

Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).
Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note: 3. NC balls may be mated with any solder pad on PCB.
Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

Exhibit 66

PCB Pad Array Options for SDRAM Placements

MO-207 Variation DW-z allows any of the support balls locations to be non-populated. Many raw cards use the 72-pad array and thus support DRAM with four mechanical balls attached. The number of pads actually used is dependent on the package size of the DRAMs applied to the module. The 68-pad array corresponds with MO-207 Variation DT-z.
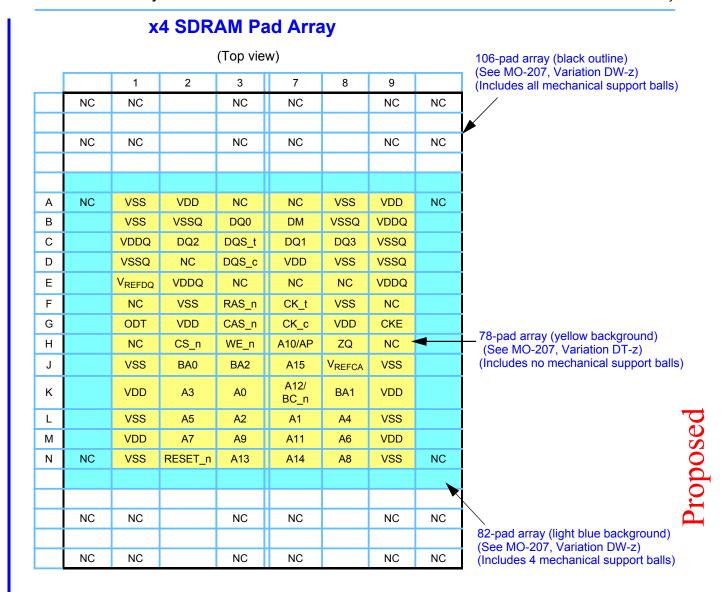
There are five basic pad arrays: x4 pad array, x8 pad array, x4 pad array DDP stacked, x8 pad array DDP stacked and x4 pad array QDP stacked. Each of these pad arrays may have a ball count variation. Below is a description of these 2 variations found on currently established raw card reference designs:

- 78-pad array (Variation DT-z, or DW-z with no support balls)

- 82-pad array (Variation DW-z with 4 support balls)

Proposed

Exhibit 66

x4 SDRAM Pad Array

(Top view)

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

	1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V_{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		NC	VSS	RAS_n	CK_t	VSS	NC	
G		ODT	VDD	CAS_n	CK_c	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V_{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

78-pad array (yellow background)
 (See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.
Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.
Note: 3. NC solder pads may be mated with any balls of an SDRAM.

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
x8 SDRAM Pad Array

x8 SDRAM Pad Array

(Top view)

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V$_{REFDQ}$	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		NC	VSS	RAS_n	CK_t	VSS	NC	
G		ODT	VDD	CAS_n	CK_c	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V$_{REFCA}$	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.
Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.
Note: 3. NC solder pads may be mated with any balls of an SDRAM.

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
x4 SDRAM Pad Array DDP Stacked

x4 SDRAM Pad Array DDP Stacked

(Top view)

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

	1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V_{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V_{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.
Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.
Note: 3. NC solder pads may be mated with any balls of an SDRAM.

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
x8 SDRAM Pad Array DDP Stacked   JEDEC internal use only

x8 SDRAM Pad Array DDP Stacked

(Top view)

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

	1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V_{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V_{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.
Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.
Note: 3. NC solder pads may be mated with any balls of an SDRAM.

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
 x4 SDRAM Pad Array QDP Stacked   JEDEC internal use only

x4 SDRAM Pad Array QDP Stacked

(Top view)

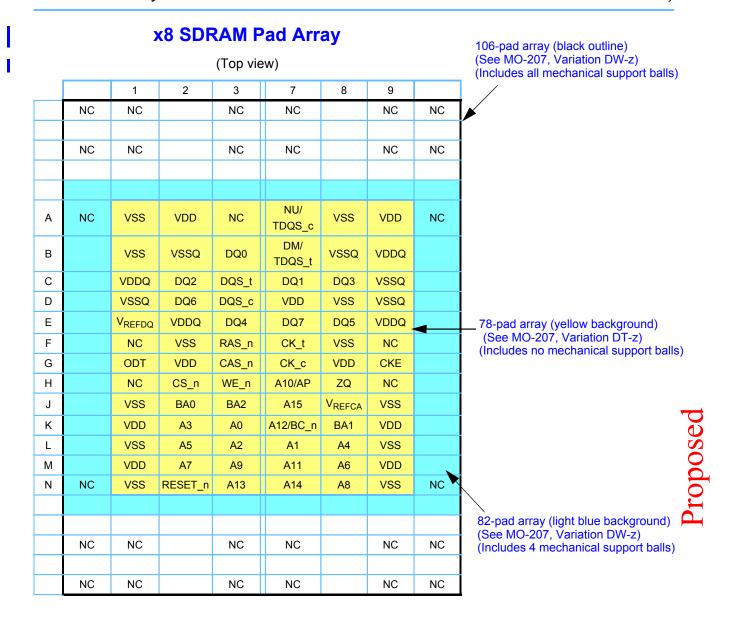|		1	2	3	7	8	9	
	NC	NC			NC	NC		NC	NC
	NC	NC			NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V_{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V_{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC			NC	NC		NC	NC
	NC	NC			NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Exhibit 66

x8 SDRAM Pad Array QDP Stacked

(Top view)

	1	2	3	7	8	9	
NC	NC		NC	NC		NC	NC
NC	NC		NC	NC		NC	NC
A　NC	VSS	VDD	NC	NU/TDQS_c	VSS	VDD	NC
B	VSS	VSSQ	DQ0	DM/TDQS_t	VSSQ	VDDQ	
C	VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D	VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E	V_{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F	ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G	ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H	CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J	VSS	BA0	BA2	A15	V_{REFCA}	VSS	
K	CS2_n	A3	A0	A12/BC_n	BA1	ZQ2	
L	CS3_n	A5	A2	A1	A4	ZQ3	
M	VDD	A7	A9	A11	A6	VDD	
N　NC	VSS	RESET_n	A13	A14	A8	VSS	NC
NC	NC		NC	NC		NC	NC
NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Exhibit 66

Pin Assignments for Memory Buffer

Memory Buffer (Top View)
588-Ball TFBGA 0.65 x 0.65 mm pitch [MO-XXX Variation X]

Left Side (1 of 3)

	A	B	C	D	E	F	G	H	J	K	L	M	N
20	NB	NB	VSS	DQ7	DQS9_t	DQ2	DQ3	VDD	DQ68	DQS17_t	DQ70	VSS	DQ66
19	NB	VSS	DQ4	DQ6	DQS9_c	VSS	DQ1	VSS	DQ69	DQS17_c	DQ71	VSS	DQ67
18	VSS	VDD	VSS	DQ5	DQS0_c	DQ0	NB	NB	NB	NB	NB	DQS8_t	DQ64
17	MDQ5	MDQ4	MDQ0	VSS	DQS0_t	VSS	NB	NB	NB	NB	NB	DQS8_c	DQ65
16	MDQS9_t	MDQS9_c	MDQS0_c	MDQS0_t	VDD	QACAS_n	NB	NB	NB	NB	NB	VDD	VDD
15	MDQ6	MDQ7	MDQ2	MDQ1	VDD	QARAS_n	NB	NB	NB	NB	NB	QAECC2	QAECC6
14	VSS	VSS	VSS	MDQ3	VDD	QAA15	NB	NB	NB	NB	NB	VDD	VDD
13	DQS1_t	DQS1_c	VSS	VDD	QAA10	QACKE1	NB	NB	NB	NB	NB	QAWE_n	VDD
12	VDD	VSS	DQ8	VDD	QACKE0	QAA12	NB	NB	NB	NB	NB	QABA0	QABA2
11	DQ11	DQ10	DQ9	VDD	QABA1	QACKE2	NB	NB	NB	NB	NB	QAA0	VDD
10	DQ15	DQ14	DQ13	VDD	QACKE3	QAA4	NB	NB	NB	NB	NB	QAA3	QACS0_n QCS0_n
9	VDD	VSS	DQ12	VDD	QAA1	QAA5	NB	NB	NB	NB	NB	QACS3_n QCS3_n	QACS2_n QCS2_n
8	DQS10_t	DQS10_c	VSS	VDD	VDD	QAA11	NB	NB	NB	NB	NB	QAA5	QAA2
7	VSS	VSS	VSS	MDQ9	VDD	QAA8	NB	NB	NB	NB	NB	QA13	QAA9
6	MDQ12	MDQ13	MDQ8	MDQ11	VDD	QAA14	NB	NB	NB	NB	NB	QAA7	VDD
5	MDQS10_t	MDQS10_c	MDQS1_c	MDQS1_t	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS
4	MDQ14	MDQ15	MDQ10	VSS	DQS2_t	DQ16	NB	NB	NB	NB	NB	MDQS2_c	VSS
3	VSS	VDD	VSS	DQ19	DQS2_c	DQ17	NB	NB	NB	NB	NB	MDQS2_t	VSS
2	NB	VSS	DQ18	DQ22	DQS11_c	DQ20	VSS	MDQ20	MDQS11_c	MDQ22	VSS	MDQ16	MDQ18
1	NB	NB	VSS	DQ23	DQS11_t	DQ21	VSS	MDQ21	MDQS11_t	MDQ23	VSS	MDQ17	MDQ19
	A	B	C	D	E	F	G	H	J	K	L	M	N

Proposed

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
 Pin Assignments for Memory Buffer   JEDEC internal use only

Middle (2 of 3)

	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE
20	VDD	Y3_c	Y3_t	Y1_t	Y1_c	Y2_c	Y2_t	Y0_t	Y0_c	VDD	ZQ	SCL
19	VDD	VSS	PVDD	VSS	PVDD	VSS	PVDD	VSS	PVDD	VSS	ZQVSS	SDA
18	VSS	MDQ68	MDQS17_t	MDQ70	MDQ64	MDQS8_c	MDQ66	VSS	CK_t	CK_c	VSS	VDD
17	VSS	MQD69	MDQS17_c	MDQ71	MDQ65	MDQS8_t	MDQ67	TEST(0)	AVSS	AVDD	AOUT	TEST(2)
16	VDD	VSS	VDD	VSS	VDD	VSS	VDD	TEST(1)	VDD	VSS	VDD	VSS
15	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
14	QAECC9	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
13	QAODT1	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	QBCKE1
12	QAODT0	VSS	RESET_n	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	QBCKE0
11	VSS	VDD	DCKE2	VDD	DA1	VDD	VSS	DCS2_n	DCS4_n	DCS3_n	VSS	QBCKE3
10	QACS1_n QSC1_n	QRST_n	DCKE1	DA12	DA6	DA4	DA2	DA13	DCS0_n	DCS5_n	DBA1	VDD
9	VDD	DCKE0	DBA2	DA11	DA3	DA5	PAR_IN	DODT0	DA0	DBA0	DODT1 DCKE3	VSS
8	VDD	DA15	DA14	DA9	DA8	DA7	DCS1_n	DCAS_n	DRAS_n	DA10	DCS6_n	DCS7_n
7	VDD	VDD	ERROUT_n	VDD	VDD	VDD	VDD	VDD	VDD	DWE_n	VDD	VDD
6	DQ24	DQ25	VSS	MDQ29	MDQS12_t	VSS	MDQ36	MDQS13_t	MDQ37	VSS	DQ32	DQ33
5	DQS3_t	DQS3_c	VSS	MDQ30	MDQS12_c	MDQ28	VSS	MDQS13_c	MDQ38	VSS	DQS4_t	DQS4_c
4	DQ26	DQ27	VSS	MDQ31	MDQS3_c	VSS	MDQ32	MDQS4_c	MDQ39	VSS	DQ34	DQ35
3	VDD	DQ28	DQ29	VSS	MDQS3_t	MDQ24	VSS	MDQS4_t	VSS	DQ36	DQ37	VDD
2	VSS	DQS12_t	DQS12_c	VSS	MDQ25	VSS	MDQ33	MDQ34	VSS	DQS13_t	DQS13_c	VSS
1	VSS	DQ30	DQ31	VSS	MDQ26	MDQ27	VSS	MDQ35	VSS	DQ38	DQ39	VSS
	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE

Proposed

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
 Pin Assignments for Memory Buffer   JEDEC internal use only

Right Side (3 of 3)

	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV
20	SA2	SA0	QVREFCA	VDD	QVREFDQ	VDD	DQ59	DQ58	DQS7_t	DQ63	VSS	NB	NB
19	VCCSPD	SA1	VREFCA	VSS	VREFDQ	VSS	DQ57	VSS	DQS7_c	DQ62	DQ60	VSS	NB
18	EVENT_n	BFUNC	NB	NB	NB	NB	NB	DQ56	DQS16_c	DQ61	VSS	VDD	VSS
17	VSS	VDD	NB	NB	NB	NB	NB	VSS	DQS16_t	VSS	MDQ58	MDQ63	MDQ62
16	VDD	VSS	NB	NB	NB	NB	NB	QBWE_n	VDD	MDQS7_t	MDQS7_c	MDQS16_c	MDQS16_t
15	QBCAS_n	QBRAS_n	NB	NB	NB	NB	NB	QBBA0	VDD	MDQ59	MDQ57	MDQ61	MDQ60
14	VDD	VDD	NB	NB	NB	NB	NB	QBA0	VDD	MDQ56	VSS	VSS	VSS
13	QBA10	QBA15	NB	NB	NB	NB	NB	QBA3	QBODT1	VDD	VSS	DQS6_c	DQS6_t
12	VDD	VDD	NB	NB	NB	NB	NB	QBA2	QBBA2	VDD	DQ48	VSS	VDD
11	QBBA1	QBA12	NB	NB	NB	NB	NB	QBA5	QBODT0	VDD	DQ49	DQ50	DQ51
10	QBCKE2	QBA4	NB	NB	NB	NB	NB	QBCS1_n QCS5_n	QBCS0_n QCS4_n	VDD	DQ53	DQ54	DQ55
9	QBA1	QBA6	NB	NB	NB	NB	NB	QBCS3_n QCS7_n	QBCS2_n QCS6_n	VDD	DQ52	VSS	VDD
8	VDD	VDD	NB	NB	NB	NB	NB	QBA9	VDD	VDD	VSS	DQS15_c	DQS15_t
7	QBA11	QBA8	NB	NB	NB	NB	NB	QBA13	VDD	MDQ51	VSS	VSS	VSS
6	VDD	QBA14	NB	NB	NB	NB	NB	QBA7	VDD	MDQ49	MDQ50	MDQ55	MDQ54
5	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS	MDQS6_t	MDQS6_c	MDQS15_c	MDQS15_t
4	VSS	MDQS5_c	NB	NB	NB	NB	NB	DQ40	DQS5_t	VSS	MDQ48	MDQ53	MDQ52
3	VSS	MDQS5_t	NB	NB	NB	NB	NB	DQ41	DQS5_c	DQ45	VSS	VDD	VSS
2	MDQ40	MDQ43	VSS	MDQ44	MDQS14_t	MDQ47	VSS	DQ42	DQS14_c	DQ46	DQ44	VSS	NB
1	MDQ41	MDQ42	VSS	MDQ45	MDQS14_c	MDQ46	VSS	DQ43	DQS14_t	DQ47	VSS	NB	NB
	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV

Proposed

Exhibit 66

Pin Assignments for Serial Presence Detect

(MO-229 Variation V/WCED-3, 2x3 mm package, 8 lead DFN 0.5 mm pitch)
(MO-229 Variation V/WEED-7, 3x3 mm package, 8 lead DFN 0.5 mm pitch)
256-byte Serial Presence Detect device, TSE2002 with thermal sensor

SPD Pinout (Top view)

TSE2002			
1	SA0	VDDSPD	8
2	SA1	EVENT	7
3	SA2	SCL	6
4	VSSSPD	SDA	5

Note: 1. Above rotations of leads correspond to footprints on PCB.
Note: 2. Refer to *JESD21C-4.1.2 -- SERIAL PRESENCE DETECT STANDARD, General Standard* for landing pattern details.

Proposed

Exhibit 66

DDR3 Load Reduced DIMM Wiring Details

Signal Groups

This specification categorizes tiiming-critical signals into eight groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group
Clock Driver Input / Unused Clocks	CK0_t, CK0_c / CK1_t, CK1_c
Clock Driver Output	Yx_t, Yx_c
Pre-MB Data, DQS_t, DQS_c	DQ[63:0],CB[7:0],DQS[17:0_t],DQS[17:0]_c, DM[8:0]/TDQS[17:9]_t,TDQS[17:9]_c
Post-MB Data, MDQS_t, MDQS_c	MDQ[71:0],MDQS[17:0_t],MDQS[17:0]_c,
Pre-MB Address and Control (Chip Select, Clock Enable, Parity, ODT)	A[15:0], BA[2:0], RAS_n, CAS_n, WE_n CS[3:0]_n, CKE[1:0], Par_In, ODT[1:0]
Post-MB Address and Control	QA[15..0], QBA[2..0], QRAS_n, QCAS_n, QWE_n, QCS[3:0]_n, QCKE[1:0], QODT[1:0]
Address and Command Parity	ErrOut_n
RESET_n	RESET_n

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing guidelines are as follows

- Route all signal traces except clocks using minimum of 0.075/0.1 rules, i.e., 0.075 mm traces and 0.1 mm minimum spacing between adjacent traces.But spacing should be as wide as possible to prevent crosstalk.
- Route clocks using minimum of 0.075 mm lines and 0.1 mm spaces between differential clock pairs and differential DQS_t,DQS_c.
- Route clocks using at least 90% of the total trace length in the inner layers. Maximize use of internal layers for routing clocks. Surface routing should be minimized and limited to what is neccesary to connect to component.
- Signals are referenced to Vss or Vdd on adjacent layers. Data signals are referenced to Vss. Address and Command signals are referenced to VDD.
-

Proposed

Signal referencing information

Signal groups	Referencing	Signal groups	Referencing
Pre-MB DQ/DQS pair	Ground layer	Pre-MB address and command net	Vdd shape
Post-MB MDQ/MDQS pair	Ground layer	Post-MB address and command net	Vdd shape
Clock nets	Vdd shape		

Exhibit 66

Differential Clock Net Structures

CK0_t, CK0_c, Yx_t, Yx_c

DDR3 SDRAM clock signals must be carefully routed to meet the following requirements:
- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 2.54 mm total) between clocks of the same function

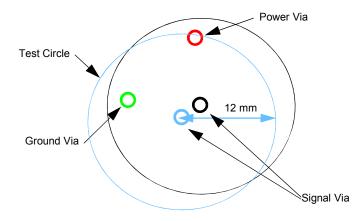Clock Driver input net segment length is newly defined and optimized for high speed DDR3 Load Reduced DIMMs.

Proposed

Exhibit 66

Test Points

All DDR3 components are in BGA packages which makes the package pads inaccessible for probing during system development. The DDR3 Registered DIMMs have test points identified to make initial evaluation easier. In some cases test pads have been added and in other cases existing vias are used as test points. An effort has been made to provide testability on some signals in all signal groups but 100% coverage is not possible. All test points must have a power and/or ground via within 12 mm. Test point location and /or availability are indicated for each raw card in the corresponding appendices.
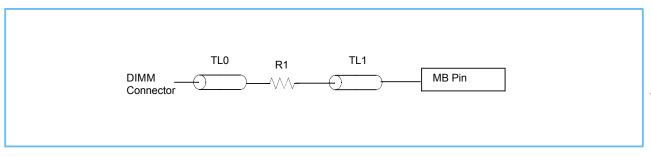
Test Point Location

Proposed

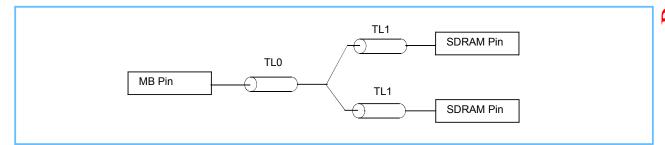Exhibit 66

Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators "TL") represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 4 GB double-sided x72 DIMM using 1 Gbit, 128Mx8 SDRAM devices would have a data net structures as shown in the following diagrams.

Exhibit 66

Timing Budgets

This section will be added following further definition of the Memory Buffer Specifications

Proposed

Exhibit 66

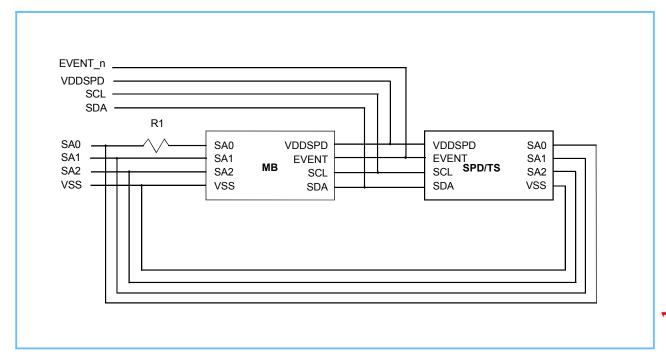## Wiring for SMBus
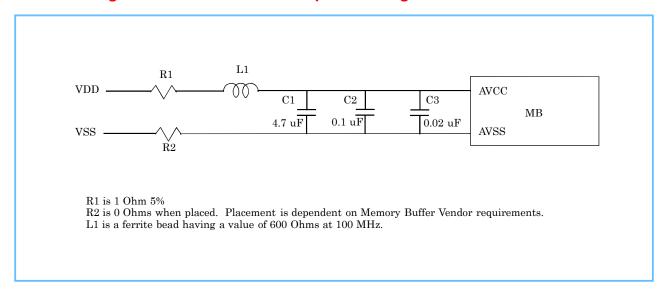
Schematic of SPD/Thermal Sensor and MB

The following schematic illustrates the required wiring of the SPD/TS and MB

This specific wiring is required. The value of R1 is typically 1K, 5% but this is a guideline. The SA0 pin may have 12 Volts applied to it for programming the SPD. Under these conditions the current into the MB must be limited. R1 serves the purpose of limiting the current into the MB.

Proposed

The following schematic defines the required wiring for AVCC.

R1 is 1 Ohm 5%
R2 is 0 Ohms when placed. Placement is dependent on Memory Buffer Vendor requirements.
L1 is a ferrite bead having a value of 600 Ohms at 100 MHz.

Exhibit 66

DIMM Wiring Requirements

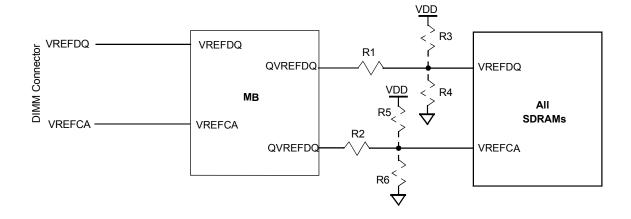These are requirements for compatibility. If deviations are required they must be identified and explained in the appropriate appendix.

All SDRAM components must have separate ZQ resistors for each pin on the SDRAM component.

The ECC byte lane as defined by the edge connector must connect to MB pins identified as DQ63 to DQ71. For the ECC byte lane there must be a one to one match in the pin ordering between the connector and the MB, CB0 to DQ63, etc. The associated strobes must also be connected one to one.

For all other byte lanes, the strobes must match the routing as defined in the table. The bits must be kept with the associated strobes. For non-ECC byte lanes and modules with x8 SDRAM components swapping bits within the byte is allowed. For non-ECC byte lanes and modules with x4 SDRAM components swapping bits within the nibble is allowed. For non-ECC byte lanes and modules with x4 SDRAM components swapping bits between nibbles is not allowed.

Gold Finger to Memory Buffer Mapping Table					
DIMM Gold Finger Connector Pin Name	Horizonal MB MB Pin Name	Vertical MB MB Pin Name	DIMM Gold Finger Connector Pin Name	Horizontal MB MB Pin Name	Vertical MB MB Pin Name
DQS0	DQS0	DQS5	DQS9	DQS9	DQS14
DQS1	DQS1	DQS2	DQS10	DQS10	DQS11
DQS2	DQS2	DQS3	DQS11	DQS11	DQS12
DQS3	DQS3	DQS4	DQS12	DQS12	DQS13
DQS4	DQS4	DQS7	DQS13	DQS13	DQS16
DQS5	DQS5	DQS1	DQS14	DQS14	DQS10
DQS6	DQS6	DQS0	DQS15	DQS15	DQS9
DQS7	DQS7	DQS6	DQS16	DQS16	DQS15
DQS8	DQS8	DQS8	DQS17	DQS17	DQS17

Proposed

As illustrated in the figure VREFCA from the edge connector must be wired to VREFCA of the MB. VREFDQ from the edge connector must be wired to VREFDQ of the MB. VREFCA and VREFDQ for the SDRAMs components must be wired to resistor dividers as illustrated with R3/R4 and R5/R6. The values of R3, R4, R5

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
 DIMM Wiring Requirements

and R6 are TBD. These are not placed on the JEDEC standard DIMM. QVREFDQ and QVREFCA from the MB must be wired to the SDRAMs through series resistors as illustrated with R1 and R2. These resistors are zero Ohms and will be placed on JEDEC standard DIMMs.

Pin 77 of the edge connector is defined as ODT1 or CKE3. It will be wired to the MB through a TBD Ohm resistor.

Pin 167 of the edge connector is defined as CKE2. For the JEDEC standard LRDIMM it is not used. It will wired to the MB through a TBD Ohm resistor.

All LRDIMMs will provide some feature to reduce capacitance at the edge connector for the DQ bus. The details of how this is done will be defined by each raw card and included in the appendix.

Proposed

Exhibit 66

Serial Presence Detect Definition

Removed for now. Will request the JEDEC office add once the SPD spec is complete.

Proposed

Exhibit 66

DDR3 DIMM Label Format

This material is provided as reference only.

DDR3 "End-User" DIMM Label Format:

The following label shall be applied to all DDR3 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

Voltage options in field 'v' describe the nominal voltage VDD of the SDRAMs and support components (excluding the SPD). Values for these voltages are 'operable' which means the device characteristics such as timing are supported at this voltage, or 'endurant' which means that the device may be powered to that voltage level without damage, however should not be used as operation is not guaranteed at the higher voltage.

ggggg eRxff PC3v-wwwwwm-aa-bb-ccd

Where:

ggggg = Module total capacity, in bytes
  256MB, 512MB, 1GB, 2GB, 4GB, etc.
eR = Number of ranks of memory installed
  1R = 1 rank of DDR3 SDRAM installed
  2R = 2 ranks
  4R = 4 ranks
xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly
  x4 = x4 organization (4 DQ lines per SDRAM)
  x8 = x8 organization
  x16 = x16 organization
v = SDRAM and support component supply voltage (VDD)
  Blank = 1.5 V operable
  L = 1.35 V operable, 1.5 V operable
  U = 1.TBD V operable, 1.TBD V endurant
wwwww = Module bandwidth in MB/s
  6400 = 6.40 GB/s (DDR3-800 SDRAMs, 8 byte primary data bus)
  8500 = 8.53 GB/s (DDR3-1066 SDRAMs, 8 byte primary data bus)
  10600 = 10.66 GB/s (DDR3-1333 SDRAMs, 8 byte primary data bus)
  12800 = 12.80 GB/s (DDR3-1600 SDRAMs, 8 byte primary data bus)
  14900 = 14.93 GB/s (DDR3-1866 SDRAMs, 8 byte primary data bus)
  17000 = 17.06 GB/s (DDR3-2133 SDRAMs, 8 byte primary data bus)
m = Module Type
  E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
  F = Fully Buffered DIMM ("FB-DIMM")
  L = Load Reduction DIMM ("LRDIMM")
  M = Micro-DIMM
  N = Mini-RDIMM
  R = Registered DIMM ("RDIMM")
  S = Small Outline DIMM ("SO-DIMM")
  U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
aa = DDR3 SDRAM CAS Latency in clocks at maximum operating frequency

Proposed

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
 DDR3 DIMM Label Format   JEDEC internal use only

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM
cc = Reference design file used for this design (if applicable)
    A = Reference design for raw card 'A' is used for this assembly
    B = Reference design for raw card 'B' is used for this assembly
    AC = Reference design for raw card 'AC' is used for this assembly
    ZZ = None of the reference designs were used for this assembly
d = Revision number of the reference design used
    0 = Initial release
    1 = First revision
    2 = Second revision
    P = Pre-release or Engineering sample
    Z = To be used when field cc = ZZ

Examples:

2GB 2Rx4 PC3-10600R-7-10-D2
        is a 2 GB DDR3 RDIMM using 2 ranks of x4 SDRAMs operational to DDR3-1333 performance
        with CAS Latency = 7 using JEDEC DDR3 SPD revision 1.0, raw card reference design file D
        revision 2 used for the assembly

1GB 1Rx4 PC3L-10600R-8-10-C1
        is a 1 GB DDR3 RDIMM using 1 rank of x4 low voltage SDRAMs, operable at 1.35 V and 1.5 V
        operable, operational to DDR3-1333 performance with CAS Latency = 8 using JEDEC DDR3
        SPD revision 1.0, raw card reference design file C revision 1 used for the assembly

1GB 2Rx8 PC3-12800E-10-10-BP
        is a 2 GB DDR3 UDIMM with x72 data bus (ECC) using 2 ranks of x8 SDRAMs operational to
        DDR3-1600 performance with CAS Latency = 10 using JEDEC DDR3 SPD revision 1.0, raw
        card reference design file B pre-release revision used for the assembly

4GB 2Rx8 PC3-8500N-8-10-ZZZ
        is a 4 GB DDR3 Mini-RDIMM using 2 ranks of x8 SDRAMs operational to DDR3-1066 perfor-
        mance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, no JEDEC standard raw
        card reference design file used for the assembly

Proposed

Exhibit 66

DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240Pin DIMM family. This material is included as reference and may be out of date. Download the latest version of MO-269 for any later updates. This information can be accessed on the worldwide web as follows:

1. Go to JEDEC official site; http://www.jedec.org.

2. Click on 'Free Standards' and enter the free download area.

3. Search by document number: 'MO-269' and download the PDF for this product family.

4. Or search by 'JEP95';'JEDEC Publication 95.' and open entire document, scroll down and select

   'MO-269' to download the PDF for this product family.

Within MO-269, several DIMM thickness variations are defined. These variations are summarized in the table below, in conjunction with examples of the types of LRDIMM components and assemblies that may be associated with each DIMM thickness range:

Maximum LRDIMM Thickness	Comments
Less than or equal to 4.00 mm	Generally associated with DIMMs produced with devices that are 1.35 mm thick or less
> 4.00 mm and less than or equal to 6.75 mm	Generally associated with DIMMs produced with devices that are greater than 1.35 mm and less than or equal to 2.70 mm thick
> 6.75 mm and less than or equal to 7.55 mm	Generally associated with DIMMs produced with devices that are greater than 2.70 mm and less than or equal to 3.10 mm thick
> 7.55 mm	Intended to cover DIMMs produced with non-standard package thicknesses, card-on-card structures or alternate solutions

Proposed

Note: Maximum DIMM thickness can be a measured maximum value, or can be calculated using the maximum component, card, label, and assembly process adders.

Exhibit 66

Design File Naming Convention

"DIMM spec"_Vrrr_RC_ LLn_YYYYMMDD.zip

Where:

DIMM spec = DIMM Specification
>   PC3-LRDIMM

V = Constant representing "Version".
rrr = First revision of raw card Appendix at time of first ballot
RC = Constant representing "Raw Card"
LL = Raw Card letter(s)
n = Raw card registration number. Only to be incremented if the file is actually posted.
YYYYMMDD = Year, month and day of release if posted or last changes if under consideration.

Notes regarding release date:

1. Date will always reflect the date of the last change. Renaming of a file does not constitute a change.
2. If for example the BOM is updated, the BOM, readme and design (zip) files all receive new dates, but the brd file remains unchanged.

Notes regarding speed upgrades:

1. If for example a new BOM is needed to upgrade a design file that accomodates a new speed such as PC3-12800 then the BOM file may be named as follows:
"DIMMspec"_Vrrr_RC_LLn_YYYYMMDD_**BOM-12800**.xls
2. BOMs may be changed or added to an existing design (zip) file without incrementing the raw card registration number. However, in this case the date designation of the design file would be incremented as shown in the following examples:
>   Example Filename: PC3-LRDIMM_V100_RC_B0_20080912.zip

Proposed

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
Revision Log
JEDEC internal use only

Revision Log

Revision Info	Page of Revision	Description of Change
Revision 0.10 20090916	ALL	Initial draft
Revision 0.11 20090930	9	Update pinout table from ballot
	11	Add table for pinout comparison between LRDIMM and RDIMM. Content of table requires review.
	17	Add QDP ballout table. Content of table requires review.
	23	Add x4 QDP Pad Array table. Content of table requires review.
	24, 25, 26	Add MB pin out table. Content of table requires review.
	35	Add place holder for AVCC schematic.
Revision 0.12 20091005 20091008	4	Added dimensions and variations to table
	11	Modified table to show only pins with differences
	12	Modified # of DRAM balls column from 72 to 82
	13-17	Change component densities in title from "512Mb to 8Gb" to "1Gb to 4Gb".
	18	Change "68-pad array" to "78 pad array"
	24-26	Updated pin assignment table
	31	Update densities in title of Net Structure Example
	35	Update schematic for AVCC
	37	Update densities in label format
	5	Removed 128 GB
	10	Updated table to reflect comparing UDIMM with LRDIMM.
	12	Removed RC K entry
Revision 0.13 20091010	38	Add Data Bus Wiring Requirements
	10	Additional changes to table comparing UDIMM to LRDIMM.
Revision 0.14 20091030	10, 11, 30, 40	Corrected typos and references
	TOC, 12	Added information for RC K
	38, 39	DIMM label updated based on latest spec with hyphen removed for LRDIMM
	36	DIMM wiring requirements updated.
Revision 0.15 20091104	6,8,9,30	Changed Err_Out_n to ErrOut_n
	4	Adjusted wording for address mirroring
	30	Chnaged placement of brackets [ ] in signal names
	36	Corrected table for Gold finger to Memory buffer mapping
	36	Changed text regarding required wiring of QVREF_DQ
	36	Change 22 Ohms to TBD Ohms
	36/37	Changed description of VTT connection to be more clear.
Revision 0.16 20091104	4	Adjusted wording related to ODT1
	29	Incorporated latest SPD pinout, text and figure
	30	Added figure for VREFDQ and VREFCA. Adjusted wording for VREFCA and VREFDQ.
	30/31	Removed text discussing VTT connections.

Exhibit 66

DDR3 SDRAM LRDIMM Design Specification
  Revision Log

Revision Info	Page of Revision	Description of Change

Proposed

Exhibit 66

EXHIBIT R
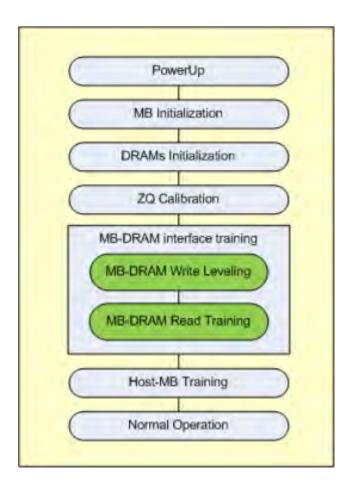
MB Initialization sequence Item 142.35

6-4-09

Exhibit 67

Where Semiconductor Leaders Set Standards for the World!
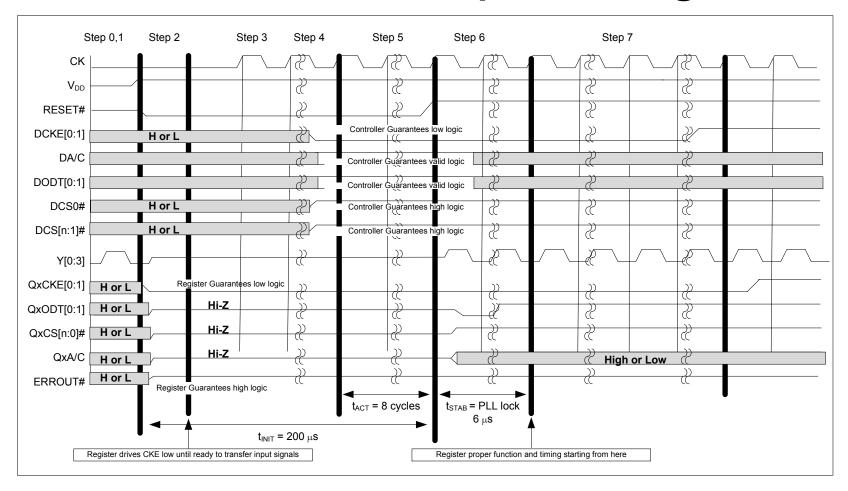
Initialization Overview

1. Power up requirements same as 882
2. Host initializes MB CWords
3. Host initializes DRAM MRS registers
4. Host issues ZQ command to DRAM
5. Host issues CWord write to start MB-DRAM interface training
6. Host does interface training
7. Normal Operation

Exhibit 67

MB Power Up Timing

Exhibit 67

MB Power Up Table

Step	#	power	input								Outputs						
			RESET#	Vref	DCK	DCKE	DCS#	DCMD	DQ/S	DODT	QxCKE	QxCK	QxCS	QxODT	QxCMD	ERROUT#	MDQ/S
No Power	0	0	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z	Z
Power Ramp	1	0->V_{DD}	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X orZ
Power Adjust	2	V_{DD} 1.5→1.35 1.35-->1.5	L	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	Z	Z	H	Z
Clock start	3	V_{DD}	L	X or Z	running	X or Z	X or Z	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Drive CKE/CS	4	V_{DD}	L	X or Z	running	L	H	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Apply Vref	5	V_{DD}	L	stable	running	L	H	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Reset release	6	V_{DD}	H	stable	running	L	H	X or Z	Z	L	L	running	H	L	X	H	Z
Normal operation	7	V_{DD}	H	stable	running	X	X	X	X or Z	X	X	running	X	X	X	X	X or Z

- ❖ Power up sequence is same as 882 device
  - ❖ MB internal circuit calibration is done within the tSTAB time
- ❖ MB doesn't forward DODT as 882, instead the QxODT is initiated by MB depending on the CMD and QxODT configuration

Exhibit 67

Host RCW to Configure MB

❖ Frequency and Voltage RCW to be programmed first

❖ No specific ordering requirements for the rest

- ❖ Address Splitting Mode

- ❖ Number Input Ranks and Output Ranks

- ❖ CKE, DODT Modes

- ❖ Mirroring Mode

- ❖ QxODT values per rank.

- ❖ MRS RTT Values

- ❖ MRS Masking

❖ Each of these items has been specified in JEDEC TG showings

Exhibit 67

Host MRS to Configure DRAM

❖ Host issues ZQ commands to DRAMs

  ❖ MB doesn't intercept nor response to ZQ command

  ❖ ZQ command is forward to DRAMs

❖ Host issues MRS commands
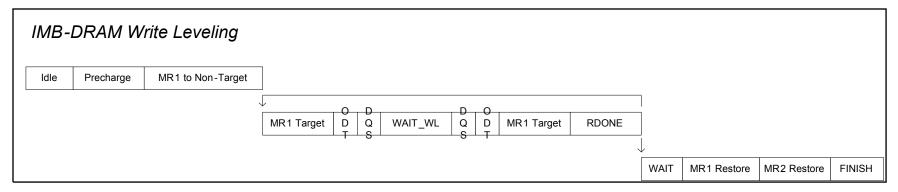
  ❖ MRS command is forward to DRAMs

Exhibit 67

MB-DRAM interface training

❖ Host writes CWord, F0RC12, to start the IMB-DRAM training and wait …

❖ MB does write leveling to DRAM

❖ MB does RxEn training to DRAM

❖ MB return to idle state and ready to start normal operation

Exhibit 67

MB-DRAM Write Level Steps

IMB-DRAM Write Leveling

Idle	Precharge	MR1 to Non-Target

MR1 Target	ODT	DQS	WAIT_WL	DQS	ODT	MR1 Target	RDONE

WAIT	MR1 Restore	MR2 Restore	FINISH
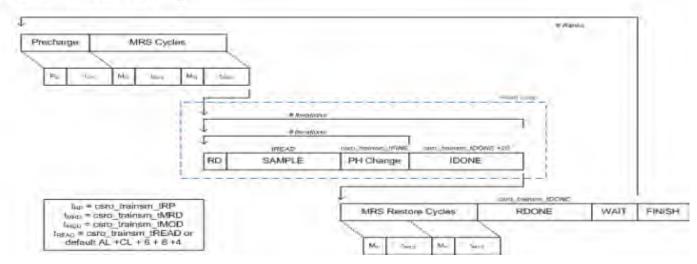
❖ Set MR1 for non-target ranks to disable the output drivers.

❖ Write Level for Target Rank per DRAM spec

1. Set MR1 A7 to 1 for target rank to enable Write Leveling
2. Send DESELECT/NOP during Write Leveling.
3. MB waits and assert QODT[x] for that rank.
4. After X nCK MB generates MDQS
5. After Y nCK, MB samples MDQ inputs.
6. MB steps through all phases for optimal MDQS phase.

❖ Repeat the write level process for each physical rank.

Exhibit 67

MB-DRAM RxEn Training Steps

IMB-DRAM Read Training

- ❖ Send PREA to the physical rank under training.
- ❖ Enable DRAM to provide data to buffer
- ❖ RxEn Training Iterations
- ❖ Repeat for each physical rank defined by number of physical rank register.

Exhibit 67

MB-DRAM Complete Training Time

❖ After enabling the IMB-DRAM training by setting F0RC12 to 010b, the Host must wait a predetermined number of cycles before moving to next step

❖ Number Cycles = WL Training Time + Read Training Time

Exhibit 67

Host-MB Training

❖ Write Level

- MB masks Host issued DRAM WL command

- Host enables Host-MB WL by writing to MB

- MB WL Timing same as DRAM

Exhibit 67

EXHIBIT S

Memory Buffer Membist for LRDIMM

DDR3 MB TG item # 142.43
June 4th, 2009

Exhibit 68

Consensus List

MB TG consensus list:

24: MB to support Transparent Mode and MemBIST. (added 01-12-09)

34. All Memory Buffers on an LRDIMM will be able to start membist using a single RCW command (added 02-16-09)

35 All Memory Buffers on an LRDIMM will be able to start membist using a single SMBus CSR write command (added 02-16-09)

Exhibit 68

Why does LRDIMM need Membist ?

- **Quick way to check for DIMM level connectivity**
  - Fully Hidden DRAM interface behind buffer
  - Memory buffer does not have boundary scan or JTAG
  - Membist exercises all pins between buffer and DRAMs
  - Transparent Mode requires special edge connector tester
  - Membist needs only power and SMBus

- **Exercise/Stress DIMM with System Level timings**
  - Membist uses the same settings the host uses
  - DRAM interface must be fully trained before membist
    - SMBus CSR write or RCW write to start training just like host
  - Results correlate with system level environment
  - Quick Debug method to determine root cause

Exhibit 68

Why does LRDIMM need Membist ? cont

Characterization, Validation, Debug and Failure Analysis

– Data Patterns, Address Patterns, failure locators

– Allows for shmooing of any parameter (V, T, F, timing, etc)

– Flexible control to stress all timings on LRDIMM

- Back 2 Back Write to Read
- Back 2 Back Read to Write
- Rank to Rank
- Etc

– Needed to determine LRDIMM SPD settings

System Level Checking and Clearing Memory in BIOS

– Similar to FBDIMM

– BIOS checks multiple DIMMs in parallel with LFSR data

- Disables Ranks / DIMMs before BOOT
- Large memory space covered in short time

– BIOS can clear ALL memory for valid ECC data

Exhibit 68

Membist Features Overview

Membist super-set to FBDIMM AMB

- Per nibble data pattern control
    - Burst user data
    - Fixed data (0, F, A, 5, etc)
    - 32 bit LFSR data pattern
    - Mats, March, etc
- All ranks included in address algorithm
    - Gapless rank interleave
    - Row, Col, Bank, Rank and Burst order control
    - Single address, Address range or Full DRAM address
- Nibble Disable (write) and Membist Compare mask
- Error indicators
- Per nibble expect data vs captured data
    - Storage for captured data failures
    - Captured data per early/late double burst
    - Error DQ location per early/late double burst
- Failing address locations captured
    - Address, captured data and DQ error stored per failure
    - Skip 0 to 2^{16} failing addresses before logging

Exhibit 68

SMBus Membist Start

Membist Started through SMBus CSR

- SMBus write to MBCSR1
- Similar Inteface to FBDIMM AMB

MBCSR1

Membist CSR #1 to specifiy the operation of Membist

Address	Register Description	Bit #	Bit Description	Type	Default
0x2F	Membist CSR1 Byte 3	7	**Start Membist** 0 = stop membist by the user, or harware will set this bit to 0 when it is done 1 = start membist	RW	0b0
		6	**Membist Failure** 0 = no failure, Membist Start bit will clear this register 1 = hardware will set this bit at completion of the membist algorithm if one or more failures is detected	RWST	0b0
		5	**Valid Results are in error CSRs** 0 = not valid, membist start clears this register 1 = after successful membist run, and results are stored, harware sets this bit	RWST	0b0
		4	**Halt on Error** 0 = normal 1 = membist engine halts on 1st error, logs all errors, sets valid bit. Resepects the SKIP_FAILURES number of errors before halting	RO	0b0
		3	**Address Inversion** Whenever this bit is enabled, Bank, Row, Column address will be inverted on alternate addresses as described in the FBDIMM MemBIST chapter, 0 = regular addressing 1 = dymanic addressing	RW	0b0
		2:0	**Algorithm** 000 = Normal command will be executed from the selection of MBCSR bits field [5:4] 001 = Scan: ^ (WD1); ^(RD2); ^ (WI3); ^ (RI4) 010 = rsvd 011 = Data Retention step I or Init: ^ (WD1) 100 = Data Retention step II: ^ (RD2) 101 = Mats +: ^(WD1); ^(RD2, WI3); v(RI4, WD5) 110 = March C-: ^(WD1); ^(RD2, WI3); ^(RI4, WD5); v(RD6, WI7); v(RI8, WD9); v(RD10); 111 = rsvd	RW	0b000

Exhibit 68

RCW Membist Start

Membist Started through RCW

– BIOS level access

– RCW FN3 RC4 and RC5

– Memory Buffer needs:

  • Number rows

  • Number columns

  • All other parameters snooped from Host MRS

RCW FN3 RC4

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0		**NUMCOL: Number of Columns**
x	x	0	1	DRAM Number of Columns	00 = CA[9:0]
x	x	1	0		01 = CA[11,9:0]
x	x	1	1		10 = CA[13,11,9:0]
					11 = rsvd
0	0	x	x		**NUMROW: Number of Rows**
0	1	x	x	DRAM Number of Rows	00 = 8,192 RA[12:0]
1	0	x	x		01 = 16,384 RA[13:0]
1	1	x	x		10 = 32,768 RA[14:0]
					11 = 65,536 RA[15:0]

RCW FN3 RC5

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	reserved	
x	x	x	1		
x	x	0	x	Membist Algo	0 = fixed Data 0's, Full MTR, write full, read empty, compare, default XYZR order, all physical ranks
x	x	1	x		1 = LFSR data, Full MTR, write full, read empty,
x	0	x	x	reserved	
v	1	x	x		
0	x	x	x	Membist Start	0 = Stop membist, or membist has completed. RCW method can only write to this bit, but SMBus can observe this bit.
1	x	x	x		

Exhibit 68

SMBus Function 3 and Function 5

Function 3: JEDEC DRAM Bus Interface Registers

Legend:
- Read Only
- JEDEC Common
- MB Vendor Specific
- Reserved

Col 1	Col 2	Col 3	Col 4	Addr
DID		VID		00h
Reserved	REG_CTRL	0b0011,SA[3:0]	RID	04h
DRAM_TRFC		AREF_TREFI		08h
DSREFTC				0Ch
DRAM_TIMING				10h
DRAM_CTRL				14h
DRAM_FN_CTRL		MTR_CTRL		18h
BANK_ORDER				1Ch
DRAM_ORDER		DRAM_OPCODE		20h
Reserved	VREF_DQ	VREFOUT_CA	VREFOUT_DQ	24h
REF_RANK_CNT	REF_JITTER	REF_STAGGER	Y_CLK_DISABLE	28h
MBCSR1				2Ch
RANK_ORDER				30h
PWR_DN_CTRL				34h
PWR_DN_UP_TIMING				38h
BRST_3	BRST_2	BRST_1	BRST_0	3Ch
BRST_7	BRST_6	BRST_5	BRST_4	40h
LFSR_SEED				44h
SKIP_FAILURES		BYTE_ERR_ACCUM		48h
Reserved	Reserved	END_ADDR_MSB	ST_ADDR_MSB	4Ch
ST_ADDR_LSB				50h
END_ADDR_LSB				54h
Reserved	Reserved	FAIL2_ADDR_MSB	FAIL1_ADDR_MSB	58h
FAIL1_ADDR_LSB				5Ch
FAIL2_ADDR_LSB				60h
Reserved	Reserved	FAIL4_ADDR_MSB	FAIL3_ADDR_MSB	64h
FAIL3_ADDR_LSB				68h
FAIL4_ADDR_LSB				6Ch
Reserved	Reserved	FAIL6_ADDR_MSB	FAIL5_ADDR_MSB	70h
FAIL5_ADDR_LSB				74h
FAIL6_ADDR_LSB				78h
Reserved	Reserved	FAIL8_ADDR_MSB	FAIL7_ADDR_MSB	7Ch
FAIL7_ADDR_LSB				80h
FAIL8_ADDR_LSB				84h
NB_9_0_BIT_INV	NB_9_0_RX_MSK	NB_9_0_CTRL	NB_9_0_DAT_PAT	88h
NB_9_0_ERR_CNT		NB_9_0_ERR_ACCUM		8Ch
NB_9_0_CAPTURE_1		NB_9_0_ERROR_1		90h
NB_9_0_CAPTURE_2		NB_9_0_ERROR_2		94h
NB_9_0_CAPTURE_3		NB_9_0_ERROR_3		98h
NB_9_0_CAPTURE_4		NB_9_0_ERROR_4		9Ch
NB_10_1_BIT_INV	NB_10_1_RX_MSK	NB_10_1_CTRL	NB_10_1_DAT_PAT	A0h
NB_10_1_ERR_CNT		NB_10_1_ERR_ACCUM		A4h
NB_10_1_CAPTURE_1		NB_10_1_ERROR_1		A8h
NB_10_1_CAPTURE_2		NB_10_1_ERROR_2		ACh
NB_10_1_CAPTURE_3		NB_10_1_ERROR_3		B0h
NB_10_1_CAPTURE_4		NB_10_1_ERROR_4		B4h
NB_11_2_BIT_INV	NB_11_2_RX_MSK	NB_11_2_CTRL	NB_11_2_DAT_PAT	B8h
NB_11_2_ERR_CNT		NB_11_2_ERR_ACCUM		BCh
NB_11_2_CAPTURE_1		NB_11_2_ERROR_1		C0h
NB_11_2_CAPTURE_2		NB_11_2_ERROR_2		C4h
NB_11_2_CAPTURE_3		NB_11_2_ERROR_3		C8h
NB_11_2_CAPTURE_4		NB_11_2_ERROR_4		CCh
NB_12_3_BIT_INV	NB_12_3_RX_MSK	NB_12_3_CTRL	NB_12_3_DAT_PAT	D0h
NB_12_3_ERR_CNT		NB_12_3_ERR_ACCUM		D4h
NB_12_3_CAPTURE_1		NB_12_3_ERROR_1		D8h
NB_12_3_CAPTURE_2		NB_12_3_ERROR_2		DCh
NB_12_3_CAPTURE_3		NB_12_3_ERROR_3		E0h
NB_12_3_CAPTURE_4		NB_12_3_ERROR_4		E4h
NB_13_4_BIT_INV	NB_13_4_RX_MSK	NB_13_4_CTRL	NB_13_4_DAT_PAT	E8h
NB_13_4_ERR_CNT		NB_13_4_ERR_ACCUM		ECh
NB_13_4_CAPTURE_1		NB_13_4_ERROR_1		F0h
NB_13_4_CAPTURE_2		NB_13_4_ERROR_2		F4h
NB_13_4_CAPTURE_3		NB_13_4_ERROR_3		F8h
NB_13_4_CAPTURE_4		NB_13_4_ERROR_4		FCh

Function 5: JEDEC DFx Registers

Legend:
- Read Only
- JEDEC Common
- MB Vendor Specific
- Reserved

Col 1	Col 2	Col 3	Col 4	Addr
DID		VID		00h
Reserved	REG_CTRL	0b0101,SA[3:0]	RID	04h
				08h
				0Ch
				10h
				14h
				18h
				1Ch
				20h
				24h
				28h
				2Ch
				30h
				34h
				38h
				3Ch
		TRANS_CFS_DQ	TRANS_CFG_CA	40h
				44h
				48h
				4Ch
				50h
				54h
				58h
				5Ch
				60h
				64h
				68h
				6Ch
				70h
				74h
				78h
				7Ch
				80h
				84h
NB_14_5_BIT_INV	NB_14_5_RX_MSK	NB_14_5_CTRL	NB_14_5_DAT_PAT	88h
NB_14_5_ERR_CNT		NB_14_5_ERR_ACCUM		8Ch
NB_14_5_CAPTURE_1		NB_14_5_ERROR_1		90h
NB_14_5_CAPTURE_2		NB_14_5_ERROR_2		94h
NB_14_5_CAPTURE_3		NB_14_5_ERROR_3		98h
NB_14_5_CAPTURE_4		NB_14_5_ERROR_4		9Ch
NB_15_6_BIT_INV	NB_15_6_RX_MSK	NB_15_6_CTRL	NB_15_6_DAT_PAT	A0h
NB_15_6_ERR_CNT		NB_15_6_ERR_ACCUM		A4h
NB_15_6_CAPTURE_1		NB_15_6_ERROR_1		A8h
NB_15_6_CAPTURE_2		NB_15_6_ERROR_2		ACh
NB_15_6_CAPTURE_3		NB_15_6_ERROR_3		B0h
NB_15_6_CAPTURE_4		NB_15_6_ERROR_4		B4h
NB_16_7_BIT_INV	NB_16_7_RX_MSK	NB_16_7_CTRL	NB_16_7_DAT_PAT	B8h
NB_16_7_ERR_CNT		NB_16_7_ERR_ACCUM		BCh
NB_16_7_CAPTURE_1		NB_16_7_ERROR_1		C0h
NB_16_7_CAPTURE_2		NB_16_7_ERROR_2		C4h
NB_16_7_CAPTURE_3		NB_16_7_ERROR_3		C8h
NB_16_7_CAPTURE_4		NB_16_7_ERROR_4		CCh
NB_17_8_BIT_INV	NB_17_8_RX_MSK	NB_17_8_CTRL	NB_17_8_DAT_PAT	D0h
NB_17_8_ERR_CNT		NB_17_8_ERR_ACCUM		D4h
NB_17_8_CAPTURE_1		NB_17_8_ERROR_1		D8h
NB_17_8_CAPTURE_2		NB_17_8_ERROR_2		DCh
NB_17_8_CAPTURE_3		NB_17_8_ERROR_3		E0h
NB_17_8_CAPTURE_4		NB_17_8_ERROR_4		E4h
				E8h
				ECh
				F0h
				F4h
				F8h
				FCh

Exhibit 68

Request

- Make Motion to Authorize the MB TG task group permission to issue one or more ballots on Membist for the LRDIMM Memory Buffer

Exhibit 68

EXHIBIT T

License Assurance/Disclosure Form

PART 1

Date: February 23, 2012

Entity Name: Netlist, Inc.

Address: 51 Discovery, Suite 150

Irvine, CA 92618

IPR Contact: Jayesh Bhakta

Phone: 949-435-0025

E-Mail: jbhakta@netlist.com

PART 2

Identify the relevant JEDEC Standard:

JC40 – DDR3/ DDR4 LRDIMM components (RCD & DB) protocol and functionality module

JC42 – DDR4 3DS DRAM: JC45 – DDR4 LRDIMM

PART 3

For Issued Patents:

Patent No.: 8,081,535

Patent Name or Title: Circuit for providing chip select signals to plurality of ranks of DDR ....

Country of Issuance: USA

For Published Patent Applications:

Published Patent Application No.: _____

Patent Application Name or Title: _____

Country of Filing: _____

For Unpublished Patent Applications:

Subject Matter of Patent Application:

(See JM21P, 8.2.3 and 8.2.5 of the JEDEC Patent Policy for additional details)

License Assurance/Disclosure Form

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

PART 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

☐ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

☑ (ii) A license will be offered to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

PART 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

Jayesh Bhakta
(Signature)

February 23, 2012
(Date)

Jayesh Bhakta
(Name printed)

NOTE: The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

**RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG**

License Assurance/Disclosure Form

PART 1

Date: February 23, 2012

Entity Name: Netlist, Inc.

Address: 51 Discovery, Suite 150

Irvine, CA 92618

IPR Contact: Jayesh Bhakta

Phone: 949-435-0025

E-Mail: jbhakta@netlist.com

PART 2

Identify the relevant JEDEC Standard:

JC40 – DDR3/ DDR4 LRDIMM components (RCD & DB) protocol and functionality module

JC42 – DDR4 3DS DRAM;   JC45 – DDR4 LRDIMM

PART 3

For Issued Patents:

Patent No.: 8,081,537

Patent Name or Title: Circuit for providing chip select signals to a plurality of rank of DDR ....

Country of Issuance: USA

For Published Patent Applications:

Published Patent Application No.: _____

Patent Application Name or Title: _____

Country of Filing: _____

For Unpublished Patent Applications:

Subject Matter of Patent Application:

_____

_____

(See JM21P, 8.2.3 and 8.2.5 of the JEDEC Patent Policy for additional details)

License Assurance/Disclosure Form

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

PART 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

☐ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*

☑ (ii) A license will be offered to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

PART 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

_____

_____

IPR Contact: _____

Phone: _____

E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

Jayesh Bhakta (Signature)

February 23, 2012
_____
(Date)

Jayesh Bhakta
_____
(Name printed)

NOTE: The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

**RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG**